Quality & Reliability Monitoring Program

Quarterly Report
Ending December 2009

Zarlink's Commitment to You

We at Zarlink Semiconductor are committed to Customer Satisfaction through quality processes, products, and service.

Product quality and reliability are built into every Zarlink product from initial design to final packaging. When a product makes its way into production, ongoing quality and reliability monitoring programs are established, samples are taken from selected device families, process technologies, and finished package technologies. The Quality and Reliability Monitoring Program (RMP) Periodic Report will provide this information in which Zarlink collects on a continual basis as qualification, production, and reliability monitors are completed.

Overview

This document will be published quarterly with year-to-date data presented in a clear and concise manner. Data compiled will be shown and the proper mathematical adjustments will be made with the techniques shown within this report to deliver functional information. Results for each quarter will be shown as well as the cumulative, year-to-date results; the fourth quarter RMP report will culminate in a year-end report.

The Quality and Reliability Monitoring Program (RMP) Periodic Report will publish these results to our customers and stakeholders as an overview of our latest quality and reliability performance data. Our goal by providing these quarterly reports is to help our customers reduce and even eliminate special events for product validation through the utilization of the results communicated on a regular basis. Through this document, we aim to demonstrate Zarlink's commitment to customer satisfaction, a quality product with a high degree of reliability, and provide the high level of confidence that our customers have come to expect from us.

Any failures are used to drive our Quality Organization forward to make all necessary corrections in our patented products, processes, and technologies. We hope you find this report helpful. Please let us know if you have any specific questions or suggestions of how we may serve you better.

This report will provide the following information:

- Average outgoing quality level – AOQL
- Estimates of shipped product quality
- Reliability monitoring results
    - High temperature operating estimates- Early and Extended life
        - Failures in Time
    - Simulation of mounting on PCB- Preconditioning
    - Accelerated exposure to moisture- Autoclave

Quality Assurance Program

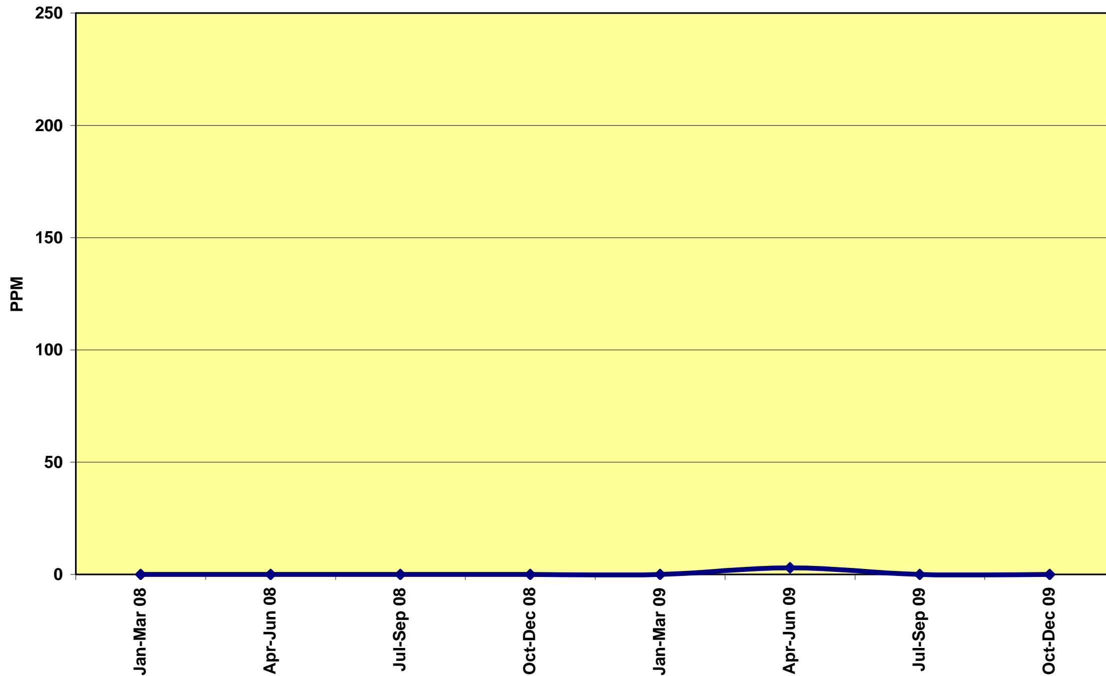
Quality is a set of attributes that characterize a device as good or bad, at time of delivery, regardless of meeting the manufacturer's or customers' specifications. The failures are generally expressed in Defects per million (DPM), Parts per million (PPM), or defective parts per million (DPPM).

Quality defects are generalized into two basic sets – Electrical and Visual/Mechanical. An Electrical failure is often most critical of the failure types and the most difficult to control. These types of failures are most likely found by stress aging.

Quality Assurance Data

The Calculated October 2009 to December 2009 AOQ per JEDEC JESD16-A is stated below:

Electrical AOQ = 0 ppm   Visual Mechanical = 0 ppm (Not Shown)



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Reliability Monitoring Program

Reliability is defined as a function over time in response to varied (specified) state condition. Reliability in this report is shown in Failure in time (FIT). One FIT represents "ONE FAILURE IN ONE BILLION DEVICE HOURS".

The Reliability Monitoring Program (RMP) at Zarlink Semiconductor is designed to provide a real-time continuous monitor of reliability performance of Zarlink integrated circuits. This program encompasses a broad range of technologies and products, and furnishes failure rate data that can be used to evaluate long-term performance.

Where not covered by external subcontractor monitoring data, Device and Package monitoring activities are performed on package and wafer fab process types to maximize data usefulness to the end user. All testing is done according to the applicable methods of JESD659 and JESD47 to ensure conformance with generally accepted practices.

Reliability Monitor Test Methodology

The standard monitoring stresses, the major failure modes that they screen, and the critical device characteristics are shown in Table 1 below. Note that additional monitors may be added to, or substituted for the following, for some or all devices, based on actual failure mechanisms observed during the course of the monitoring program. Similarly, some monitors may be excluded based on historical data and subcontractor screening for certain technologies and technology families.

Table 1: Monitor, Failure Mode, and Critical Features

MONITOR	*FAILURE MECHANISMS*	*CRITICAL DEVICE FEATURES*
High Temperature Operating Life (JESD22-A108)	Ionic movement, time dependant dielectric breakdown (TDDB), electromigration, activation of latent defects, and general aging mechanisms.	Wafer manufacture family (fab, minimum feature size, starting material, processing steps). Worst case devices have large number of processing steps, high power dissipation, and high thermal resistance.
Moisture Preconditioning (SMD only) (J-STD-020)	Moisture sensitivity of surface mount devices.	Molding compound, package style. Worst case devices have large die.
Autoclave (JESD22-A102)	Chemical corrosions	Molding compound, package style and wafer back-end processing. Worst case devices have large die in small packages.
Temperature Cycling (JESD22-A104)	Fatigue stress, difference of thermal expansion coefficients (die to package, or in bonds).	Molding compound and wafer back end processing. Worst case devices have large die and small die to lead frame spacing.
High Temperature Storage (JESD22-A103)	Fatigue stress, Intermetallic Compound formation, aging mechanisms, oxidation.	Molding compound, package style and wafer back-end processing.

Testing by Process Technologies

When comparing process technologies, Zarlink is primarily concerned with results from testing methods that look at a product's life cycle when exposed to High Temperature. High Temperature Operating Life (HTOL) is the stress test mainly used which adds high temperature and operating bias to the testing environment.

Testing by Packaging Technologies

When comparing packaging, Zarlink is concerned with how well the package will hold up to extreme environmental conditions. Tests used include Preconditioning followed by Autoclave and Temperature Cycle as well as High Temperature Storage for some package types.

The RMP test samples are taken from production lots on a generic basis to represent Zarlink's standard process flow for that given process or package technology. Zarlink also uses the RMP data provided by our Wafer Fabrication Suppliers and Assembly Subcontractors to assure a reliable product.

Calculating Failure Rates

Reliability is often expressed as a percentage or the number of failures in a unit of time. In this RMP report, Zarlink will express failure rate behavior as FIT or failures in one billion (10^9) device hours of operation. By applying an acceleration factor to show the effects of the experiment in more realistic terms, we can accurately apply the data into usable information so that corrective actions to improve upon our processes and products may be taken.

Accelerated Stress Testing

Since today's semiconductor devices are very reliable, failure-accelerating stress tests are needed to observe failure distributions within a reasonable time period. To interpret the results of accelerated stress testing, the accelerating effect of the stress must be well understood.

The relationship between stress and time to failure is determined by the activation energies of the dominant failure mechanisms for a given product. Activation energies have been determined from extensive stress testing. For times beyond the infant mortality period, an activation energy of 0.7eV is approximated for calculations within this report.

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Failure Rate (FIT) and MTBF Calculations

Instantaneous failure rates rapidly decrease to a low, relatively constant level. Steady-state instantaneous failure rates are expressed in units of FITs, failures in one billion hours of operation. The FIT rate can be calculated from the equation:

$$FR = \frac{X^{2}_{(2C+2)}}{2NTAF} * 10^{9}\ hours$$

Where:

$X2_{(2C+2)}$ = CHI-Square distribution factor with 2C+2 degrees of freedom
(taken from chi-square tables)
C = Total number of failures
N = Total number of devices tested
T = Test duration for each device at the given conditions
AF = Acceleration Factor

$$MTBF = \frac{10^{9}}{FR}$$

The calculation of the failure rates and MTBF values at a given condition is accomplished through the determination of the accelerating factor (AF) for that condition. The Arrhenius equation is used for high temperature operating life data.

High Temperature Operating Life data is extrapolated to lower temperatures through the use of the Arrhenius equation (shown below) with an assumed activation energy.

It is standard to report results as failure rates at the 55 degrees C life test temperature.

$$\mathrm{AF} = \frac{FR_1}{FR_2} = e^{\frac{E_a(1/t_2 - 1/t_1)}{k}}$$

Where:

FR_1 = Failure Rate at Test Condition
FR_2 = Failure Rate at Use Condition
E_a = Activation Energy
t_1 = Test Temperature in Degrees Kelvin (=temperature in degrees Celsius + 273)
t_2 = Use Temperature in Degrees Kelvin (=temperature in degrees Celsius + 273)
k = Bolzmann's Constant (=0.86 X 10^{-4} eV/Kelvin)
e = 2.718

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Standardized Stress Tests

RMP testing is conducted on products that are selected by process technology, assembly sites, and package types. Other criteria used to determine which devices are selected include strategic importance, production volume, process or product complexity, and devices that had recently undergone a corrective action.

Life Cycle Tests

High Temperature Operating Life (HTOL)

The purpose of High Temperature Operating Life (HTOL) is to simulate the end-user part application over early, inherent, or extended life period of the product, depending on the duration of the test. HTOL stresses components with high temperature while operating under higher than normal voltage. Zarlink follows the JEDEC recommended test conditions at 125°C and run for up to 1000 hours, sometimes with periodic pulls at 168 and 500 hours to look for electrical failure. The elevated temperature and voltage are used to provide sufficient acceleration at a typical system ambient of 55°C.

Early Life Failure Rate

An early life failure rate (ELFR) is the rate at which the device is expected to fail shortly after being put into service, typically within six months. An ELFR test of 168 hours is associated with test escapes, manufacturing defects, and marginal material. Zarlink's target is FIT$\leq$ 350.

Extended Life Failure Rate

The Extended Life Failure Rate looks for device failures after 1000 testing hours. This test shows the durability of a device for an extended operational life cycle. Zarlink's target is FIT < 100.

Environmental Tests

Preconditioning

The purpose of the preconditioning (PC) test is to stress the packaging system of an integrated circuit by simulating the harsh environmental conditions that a device experiences when handled by customer during shipping, storage, circuit board assembly, and cleaning operations. The intent of the PC test is to identify a device's sensitivity to moisture-induced stress that can cause die surface delamination. The JEDEC MSL3 mandated tests require parts to be subjected to 125°C bake followed by

moisture soak and three Pb-free temperature reflow cycles for Pb-free products. Devices are then evaluated for visual defects and tested for changes within electrical specifications.

Failures in the packaging such as delamination, cracks and "popcorn" caused by expanding moisture inside may not be visible with naked eye. Delamination cracks and "popcorn" can cause short-term reliability failure even though the chip initially passes an electrical test. The scanning acoustic micrography (SAM) technique is used to monitor for these types of defects.

Autoclave

The purpose of the autoclave test is to evaluate the reliability of non-hermetic (plastic) and non-laminate (BGA) integrated circuits in humid conditions. The devices are subjected to excessive temperature and humidity while under elevated atmospheric pressure. JEDEC standards specify 121°C, 100% relative humidity, and 205kPa atmospheric pressure. These conditions induce accelerated penetration of moisture through the packaging or along its interface with the leads passing through it. Devices are then evaluated for visual defects and tested for changes within electrical specifications.

Temperature Cycle

The purpose of Temperature Cycle (TC) testing is to determine the reliability of the internal circuit, packaging structure, and their solder interconnects due to exposure to many cycles between alternating high and low temperature extremes. The TC test is intended to reveal any electrical and packaging deficiencies resulting from thermal expansion mismatch between the die and the package structure. Zarlink follows the JEDEC Standard JESD22-A104 using condition B or C, for temperature cycle 1000 times, alternating between temperature extremes ranging from -55 °C to 125 °C or -65°C to 150°C respectively. These test conditions provide simulated results that compare to the extremes of storage and operation temperature to which the devices may be exposed. Devices are then evaluated for visual defects and tested for changes within electrical specifications.

High Temperature Storage

The purpose of High Temperature Storage (HTS) testing is to determine the effect on devices of long-term storage at elevated temperatures without any electrical stresses applied. Zarlink follows the JEDEC Standard JESD22-A103 condition B (150°C) for 1000 hours. Devices are then evaluated for visual defects and tested for changes within electrical specifications.

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Tin Whisker Monitoring

Most studies agree that stress is a key catalyst for whisker growth. This includes:

- Stress in the electroplated deposit and substrate.
- Degree of whiskering is proportional to the amount of compressive stress available.
- Minimizing stress in both the deposit and substrate is an objective.

In the case of tin, whisker growth is believed to depend on a combination of the tin coating and the composition of the substrate. Compressive stress in the composite substrate and coating are considered the overriding cause of whisker growth. Internal and external compressive stresses are at the root of whisker growth. For these reasons Zarlink is using a whisker mitigation procedure of annealing at 150 ^{o}C for 1 hour. The Tin Whisker Monitoring data is attached.

Solderability

The purpose of the testing is to examine the solderability of termination/external leads of the plastic packages. Zarlink follows JEDEC Standard JESD22-B102 to conduct this testing.

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Life Cycle Testing

HTOL

GLOBALFOUNDRIES (Formerly CHARTERED)

Technology	HV7 (HV8) Bipolar					
	Total Sum of Valid Fails HTOL 168	Total Sum of Sample Size HTOL 168	Total Sum of Valid Fails HTOL 500	Total Sum of Sample Size HTOL 500	Total Sum of Valid Fails HTOL 1000	Total Sum of Sample Size HTOL 1000
Cum Sample Size:	0	2270	0	1720	0	1028
Cum FIT:	168Hrs ELFR:	**31**	500Hrs FIT:	**14**	1000Hrs FIT:	**11**

Technology	HV4 Bipolar					
	Total Sum of Valid Fails HTOL 168	Total Sum of Sample Size HTOL 168	Total Sum of Valid Fails HTOL 500	Total Sum of Sample Size HTOL 500	Total Sum of Valid Fails HTOL 1000	Total Sum of Sample Size HTOL 1000
Cum Sample Size:	0	436	0	436	0	176
Cum FIT:	168Hrs ELFR:	**159**	500Hrs FIT:	**53**	1000Hrs FIT:	**66**

Technology	BCD3T					
	Total Sum of Valid Fails HTOL 168	Total Sum of Sample Size HTOL 168	Total Sum of Valid Fails HTOL 500	Total Sum of Sample Size HTOL 500	Total Sum of Valid Fails HTOL 1000	Total Sum of Sample Size HTOL 1000
Cum Sample Size:	0	1015	0	1015	0	611
Cum FIT:	168Hrs ELFR:	**68**	500Hrs FIT:	**23**	1000Hrs FIT:	**19**

Technology	0.35um (0.32um) CMOS					
	Total Sum of Valid Fails HTOL 168	Total Sum of Sample Size HTOL 168	Total Sum of Valid Fails HTOL 500	Total Sum of Sample Size HTOL 500	Total Sum of Valid Fails HTOL 1000	Total Sum of Sample Size HTOL 1000
Cum Sample Size:	2	4008	0	2004	0	2004
Cum FIT:	168Hrs ELFR:	**59**	500Hrs FIT:	**12**	1000Hrs FIT:	**6**

Technology	5/4/3um CMOS					
	Total Sum of Valid Fails HTOL 168	Total Sum of Sample Size HTOL 168	Total Sum of Valid Fails HTOL 500	Total Sum of Sample Size HTOL 500	Total Sum of Valid Fails HTOL 1000	Total Sum of Sample Size HTOL 1000
Cum Sample Size:	0	231	0	231	0	231
Cum FIT:	168Hrs ELFR:	**300**	500Hrs FIT:	**101**	1000Hrs FIT:	**50**

Technology	0.18um CMOS					
	Total Sum of Valid Fails HTOL 168	Total Sum of Sample Size HTOL 168	Total Sum of Valid Fails HTOL 500	Total Sum of Sample Size HTOL 500	Total Sum of Valid Fails HTOL 1000	Total Sum of Sample Size HTOL 1000
Cum Sample Size:	2	4384	0	1598	0	1598
Cum FIT:	168Hrs ELFR:	**54**	500Hrs FIT:	**15**	1000Hrs FIT:	**7**

Technology	HV30 Bipolar					
	Total Sum of Valid Fails HTOL 168	Total Sum of Sample Size HTOL 168	Total Sum of Valid Fails HTOL 500	Total Sum of Sample Size HTOL 500	Total Sum of Valid Fails HTOL 1000	Total Sum of Sample Size HTOL 1000
Cum Sample Size:	0	477	0	477	0	477
Cum FIT:	168Hrs ELFR:	**145**	500Hrs FIT:	**49**	1000Hrs FIT:	**24**

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HTOL

UMC

Technology	0.8um CMOS					
	Total Sum of Valid Fails HTOL 168	Total Sum of Sample Size HTOL 168	Total Sum of Valid Fails HTOL 500	Total Sum of Sample Size HTOL 500	Total Sum of Valid Fails HTOL 1000	Total Sum of Sample Size HTOL 1000
Cum Sample Size:	0	515	0	515	0	515
Cum FIT:	168Hrs ELFR:	**135**	500Hrs FIT:	**45**	1000Hrs FIT:	**23**

TSMC

Technology	0.25um CMOS					
	Total Sum of Valid Fails HTOL 168	Total Sum of Sample Size HTOL 168	Total Sum of Valid Fails HTOL 500	Total Sum of Sample Size HTOL 500	Total Sum of Valid Fails HTOL 1000	Total Sum of Sample Size HTOL 1000
Cum Sample Size:	0	900	0	900	0	900
Cum FIT:	168Hrs ELFR:	**77**	500Hrs FIT:	**26**	1000Hrs FIT:	**13**

Technology	0.18um CMOS & RFCMOS					
	Total Sum of Valid Fails HTOL 168	Total Sum of Sample Size HTOL 168	Total Sum of Valid Fails HTOL 500	Total Sum of Sample Size HTOL 500	Total Sum of Valid Fails HTOL 1000	Total Sum of Sample Size HTOL 1000
Cum Sample Size:	0	1039	0	1039	0	1039
Cum FIT:	168Hrs ELFR:	**67**	500Hrs FIT:	**22**	1000Hrs FIT:	**11**

Technology	0.13um CMOS					
	Total Sum of Valid Fails HTOL 168	Total Sum of Sample Size HTOL 168	Total Sum of Valid Fails HTOL 500	Total Sum of Sample Size HTOL 500	Total Sum of Valid Fails HTOL 1000	Total Sum of Sample Size HTOL 1000
Cum Sample Size:	0	1311	0	1311	0	1311
Cum FIT:	168Hrs ELFR:	**53**	500Hrs FIT:	**18**	1000Hrs FIT:	**9**

DALSA

Technology	1.5um (2.0um/3.0um/4.0um) CMOS					
	Total Sum of Valid Fails HTOL 168	Total Sum of Sample Size HTOL 168	Total Sum of Valid Fails HTOL 500	Total Sum of Sample Size HTOL 500	Total Sum of Valid Fails HTOL 1000	Total Sum of Sample Size HTOL 1000
Cum Sample Size:	0	546	0	546	0	546
Cum FIT:	168Hrs ELFR:	**127**	500Hrs FIT:	**43**	1000Hrs FIT:	**21**

IBM

Technology	0.5um SiGe					
	Total Sum of Valid Fails HTOL 168	Total Sum of Sample Size HTOL 168	Total Sum of Valid Fails HTOL 500	Total Sum of Sample Size HTOL 500	Total Sum of Valid Fails HTOL 1000	Total Sum of Sample Size HTOL 1000
Cum Sample Size:	0	625	0	625	0	625
Cum FIT:	168Hrs ELFR:	**111**	500Hrs FIT:	**37**	1000Hrs FIT:	**19**

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HTOL

MHS

Technology	5.0um CMOS					
	Total Sum of Valid Fails HTOL 168	Total Sum of Sample Size HTOL 168	Total Sum of Valid Fails HTOL 500	Total Sum of Sample Size HTOL 500	Total Sum of Valid Fails HTOL 1000	Total Sum of Sample Size HTOL 1000
Cum Sample Size:	0	100	0	100	0	100
Cum FIT:	168Hrs ELFR:	**694**	500Hrs FIT:	**233**	1000Hrs FIT:	**117**

Technology	4.0um CMOS					
	Total Sum of Valid Fails HTOL 168	Total Sum of Sample Size HTOL 168	Total Sum of Valid Fails HTOL 500	Total Sum of Sample Size HTOL 500	Total Sum of Valid Fails HTOL 1000	Total Sum of Sample Size HTOL 1000
Cum Sample Size:	0	326	0	326	0	326
Cum FIT:	168Hrs ELFR:	**213**	500Hrs FIT:	**71**	1000Hrs FIT:	**36**

Technology	1.5um (2.0um/3.0um) CMOS					
	Total Sum of Valid Fails HTOL 168	Total Sum of Sample Size HTOL 168	Total Sum of Valid Fails HTOL 500	Total Sum of Sample Size HTOL 500	Total Sum of Valid Fails HTOL 1000	Total Sum of Sample Size HTOL 1000
Cum Sample Size:	0	549	0	549	0	549
Cum FIT:	168Hrs ELFR:	**126**	500Hrs FIT:	**42**	1000Hrs FIT:	**21**

Technology	HG Bipolar					
	Total Sum of Valid Fails HTOL 168	Total Sum of Sample Size HTOL 168	Total Sum of Valid Fails HTOL 500	Total Sum of Sample Size HTOL 500	Total Sum of Valid Fails HTOL 1000	Total Sum of Sample Size HTOL 1000
Cum Sample Size:	1	1178	1	1178	1	1178
Cum FIT:	168Hrs ELFR:	**130**	500Hrs FIT:	**44**	1000Hrs FIT:	**22**

XFAB Germany

Technology	0.8um CMOS					
	Total Sum of Valid Fails HTOL 168	Total Sum of Sample Size HTOL 168	Total Sum of Valid Fails HTOL 500	Total Sum of Sample Size HTOL 500	Total Sum of Valid Fails HTOL 1000	Total Sum of Sample Size HTOL 1000
Cum Sample Size:	0	460	0	460	0	460
Cum FIT:	168Hrs ELFR:	**151**	500Hrs FIT:	**51**	1000Hrs FIT:	**25**

XFAB U.K.

Technology	0.35um CMOS					
	Total Sum of Valid Fails HTOL 168	Total Sum of Sample Size HTOL 168	Total Sum of Valid Fails HTOL 500	Total Sum of Sample Size HTOL 500	Total Sum of Valid Fails HTOL 1000	Total Sum of Sample Size HTOL 1000
Cum Sample Size:	0	646	0	646	0	646
Cum FIT:	168Hrs ELFR:	**107**	500Hrs FIT:	**36**	1000Hrs FIT:	**18**

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Environmental Tests

Preconditioning MSL 3 (Pb-Free Reflow)

ASE Preconditioning MSL 3 with Pb-Free Reflow	Fails/Sample Size				
	SOIC	TQFP	LQFP	PLCC	QFN
Jan-Mar 09	0/368	0/170	0/220	0/0	0/220
Apr-Jun 09	0/0	0/725	0/120	0/0	0/120
Jul-Sep 09	0/120	0/1271	0/498	0/0	0/120
Oct-Dec 09	0/120	0/77	0/527	0/416	0/274
Total	0/608	0/2243	0/1365	0/416	0/734

Autoclave (168 Hours)

ASE Autoclave (PCT) (168 hours)	Fails/Sample Size				
	SOIC	TQFP	LQFP	PLCC	QFN
Jan-Mar 09	0/80	0/30	0/30	0/0	0/30
Apr-Jun 09	0/0	0/85	0/30	0/0	0/30
Jul-Sep 09	0/30	0/30	0/30	0/0	0/30
Oct-Dec 09	0/30	0/0	0/30	0/0	0/30
Total	0/140	0/145	0/120	0/0	0/120

Temperature Cycling (1000 Cycles)

ASE Temp Cycle (1000 cycles) Condition C (-65 C/150 C)	Fails/Sample Size				
	SOIC	TQFP	LQFP	PLCC	QFN
Jan-Mar 09	0/180	0/80	0/130	0/0	0/130
Apr-Jun 09	0/0	0/86	0/30	0/0	0/30
Jul-Sep 09	0/30	0/30	0/30	0/0	0/30
Oct-Dec 09	0/30	0/0	0/107	0/0	0/106
Total	0/240	0/196	0/297	0/0	0/296

High Temperature Storage (150C, 1000 Hours)

ASE High Temp Storage (HTS) (150C, 1000 hours)	Fails/Sample Size				
	SOIC	TQFP	LQFP	PLCC	QFN
Jan-Mar 09	0/79	0/30	0/30	0/0	0/30
Apr-Jun 09	0/0	0/86	0/30	0/0	0/30
Jul-Sep 09	0/30	0/30	0/30	0/0	0/30
Oct-Dec 09	0/30	0/0	0/107	0/0	0/107
Total	0/139	0/146	0/197	0/0	0/197

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Tin Whisker Monitoring

ASEM

Ambient, Temperature Humidity, Temperature Cycling Testing

PACKAGE	PRECON	AMBIENT (30degC / 60%RH) 1500HRS	THT (55degC / 85%RH) 1500HRS	TCT (-55degC / +85degC) 500CYC
PLCC 44L (C151)	No precon(A)	Total s/size: 6 units NO WHISKERS Inspection result: 0 / 264 leads **PASS**	Total s/size: 6 units NO WHISKERS Inspection result: 0 / 264 leads **PASS**	Total s/size: 6 units NO WHISKERS Inspection result: 0 / 264 leads **PASS**
	SnPb reflow(B)	Total s/size: 6 units NO WHISKERS Inspection result: 0 / 264 leads **PASS**	Total s/size: 6 units NO WHISKERS Inspection result: 0 / 264 leads **PASS**	Total s/size: 6 units NO WHISKERS Inspection result: 0 / 264 leads **PASS**
	Pb free reflow(C)	Total s/size: 6 units NO WHISKERS Inspection result: 0 / 264 leads **PASS**	Total s/size: 6 units **MAX LENGTH : 11.20µm Inspection result: 12 / 264 leads PASS**	Total s/size: 6 units **MAX LENGTH : 14.00µm Inspection result: 8 / 264 leads PASS**
SOIC 16L (C 194)	No precon(A)	Total s/size: 6 units NO WHISKERS Inspection result: 0 / 96 leads **PASS**	Total s/size: 6 units NO WHISKERS Inspection result: 0 / 96 leads **PASS**	Total s/size: 6 units NO WHISKERS Inspection result: 0 / 96 leads **PASS**
	SnPb reflow(B)	Total s/size: 6 units NO WHISKERS Inspection result: 0 / 96 leads **PASS**	Total s/size: 6 units NO WHISKERS Inspection result: 0 / 96 leads **PASS**	Total s/size: 6 units **MAX LENGTH : 12.10µm Inspection result: 15 / 96 leads PASS**
	Pb free reflow(C)	Total s/size: 6 units NO WHISKERS Inspection result: 0 / 96 leads **PASS**	Total s/size: 6 units **MAX LENGTH : 13.30µm Inspection result: 13 / 96 leads PASS**	Total s/size: 6 units **MAX LENGTH : 18.00µm Inspection result: 22 / 96 leads PASS**
LQFP 100L (C7025)	No precon(A)	Total s/size: 6 units NO WHISKERS Inspection result: 0 / 600 leads **PASS**	Total s/size: 6 units NO WHISKERS Inspection result: 0 / 600 leads **PASS**	Total s/size: 6 units NO WHISKERS Inspection result: 0 / 600 leads **PASS**
	SnPb reflow(B)	Total s/size: 6 units NO WHISKERS Inspection result: 0 / 600 leads **PASS**	Total s/size: 6 units **MAX LENGTH : 10.43 µm Inspection result: 17 / 600 leads** **PASS**	Total s/size: 6 units **MAX LENGTH : 16.60 µm Inspection result: 25 / 600 leads** **PASS**
	Pb free reflow(C)	Total s/size: 6 units NO WHISKERS Inspection result: 0 / 600 leads **PASS**	Total s/size: 6 units **MAX LENGTH : 17.41 µm Inspection result: 22 / 600 leads PASS**	Total s/size: 6 units **MAX LENGTH : 21.50 µm Inspection result: 31 / 600 leads PASS**

Note : MAXIMUM ALLOWABLE TIN WHISKER LENGTH / GROWTH BY REFERING TO JEDEC STANDARD (JESD201).

I) Temperature Cycling **(TCT)** **- 45 µm**
II) Temperature / Humidity Storage **(Ambient)** **- 20 µm**
III) High Temperature / Humidity Storage **(THT)** **- 20 µm**

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Solderability

ASE Solderability	Fails/Sample Size				
	SOIC	TQFP	LQFP	PLCC	QFN
Jan-Mar 09	0/0	0/145	0/615	0/494	0/130
Apr-Jun 09	0/40	0/320	0/1010	0/920	0/1046
Jul-Sep 09	0/0	0/700	0/1284	0/940	0/30
Oct-Dec 09	0/20	0/460	0/1062	0/931	0/495
Total	0/60	0/1625	0/3971	0/3285	0/1701