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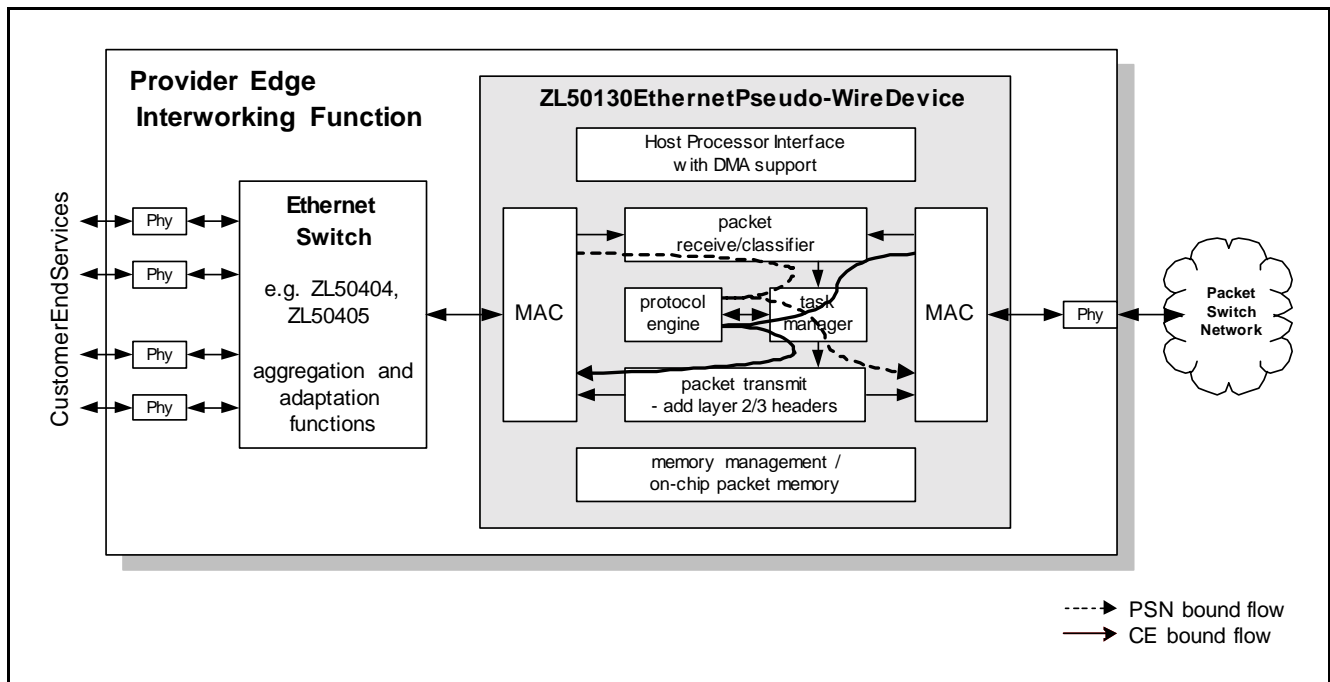
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2.0 MAC-to-MAC Applications

As an example application, the ZL50130 would be configured for MAC-to-MAC operation on a line card when connected directly to a single Ethernet switch. Figure 1 shows a ZL50130 connected to a Fast Eigabit Ethernet switch, such as the Zarlink ZL50405 Managed 5-Port 100 Mbps Ethernet Switch.

1.0 Pseudo-Wire Processor

Zarlink Semiconductor's ZL50130 is a single chip processor that performs pseudo-wire emulation edge-to-edge (PWE3) transmission. This device has three Fast Ethernet ports that perform the MAC layer function. The Fast Ethernet port is capable of operation in MII mode at 100 Mbit/s full-duplex speed. The ZL50130 device would typically interface to off-the-shelf PHYs connecting to a 100 Mbit/s Ethernet network. However, any of the MAC interfaces on the ZL50130 device may be connected directly to another MAC interface. The ability to connect two MACs directly together would eliminate the need for a PHY. This application note will detail the MAC-to-MAC interface as it applies to the ZL50130.


Figure 1 - Provider Edge Interworking Function

3.0 MII Interface Overview

The MII interface consists of a 4-bit wide data path on both receive and transmit sides. From the MAC point of view, only transmit data (TXD[3:0]) and transmit enable (TXEN) are outputs, the rest of the signals are inputs. This interface is meant to operate at 10 Mbit/s or 100 Mbit/s. The MII MAC-to-MAC connection should be configured for full duplex mode operation. For this reason, both CRS and COL are not needed for the MII MAC-to-MAC connection.

MII Signal Name	MAC Signal Direction	Description
TXD[3:0]	O	Transmit Data Bits [3:0] (driven on rising edge of TXCLK)
TXEN	O	Transmit Data Enable (indicated valid TXD[3:0])
TXCLK	I	Transmit Clock (2.5/25MHz)
RXD[3:0]	I	Receive Data Bit [3:0] (driven on rising edge of RXCLK)
RXDV	I	Receive Data Valid (indicated valid RXD[3:0])
RXCLK	I	Receive Clock (2.5/25MHz)
CRS	I	Carrier Sense (active during tx/rx activity)
COL	I	Collision Detected (asserted when collision detected in tx/rx path)

Table 1 - MII Interface Description

4.0 MII Interface Connection

This section describes the MAC-to-MAC connection for the Fast Ethernet ports on the ZL50130 when operating in MII mode at 100 Mbit/s. Table 2 details the connection between ZL50130 port 0 and a Generic MII MAC as well as the Zarlink ZL50405 Managed 5-Port 10/100M Ethernet switch. The ZL50405 can be programmed to supply TXCLK and RXCLK, thereby eliminating the need for an external per-port clock source as well as reducing the clock routing required. The Mn_REFCLK ping on the ZL50130 must be connected to the same clock source as the Mn_RXCLK on the ZL50130 for correct operation.

ZL50130 Pin Name	ZL50130 Pin Number	MII MAC Connection	ZL50408 MII MAC Connection	Notes
M_MDC	H23			No connect
M_MDIO	G26			No connect
M0_LINKUP_LED	G24			No connect
M0_ACTIVE_LED	AC26			No connect
M0_REFCLK	AA24			Connect to same clock source as M0_RXCLK.
M0_TXD[3:0]	AA23, W21, Y22, AA22	RXD[3:0]	Mn_RXD[3:0]	
M0_TXEN	V23	RXDV	Mn_CRSDV	
M0_TXCLK	U24	RXCLK	Mn_RXCLK	Connect to 25 MHz clock (100 Mbit/s) OR ZL50408 supplies clock.
M0_TXER	V22			

Table 2 - ZL50130 MII Interface Connection

ZL50130 Pin Name	ZL50130 Pin Number	MII MAC Connection	ZL50408 MII MAC Connection	Notes
M0_RXD[3:0]	W26, U22, Y26, AA26	TXD[3:0]	Mn_TXD[3:0]	
M0_RXDV	V25	TXEN	Mn_TXEN	
M0_RXCLK	AB22	TXCLK	Mn_TXCLK	Connect to 25 MHz clock (100 Mbit/s) OR ZL50408 supplies clock.
M0_RXER	V26			No connect
M0_CRS	U25			No connect (full duplex)
M0_COL	Y25			No connect (full duplex)

Table 2 - ZL50130 MII Interface Connection (continued)

Figure 2 shows the MAC-to-MAC connection between the ZL50130 and a Generic MII MAC interface.

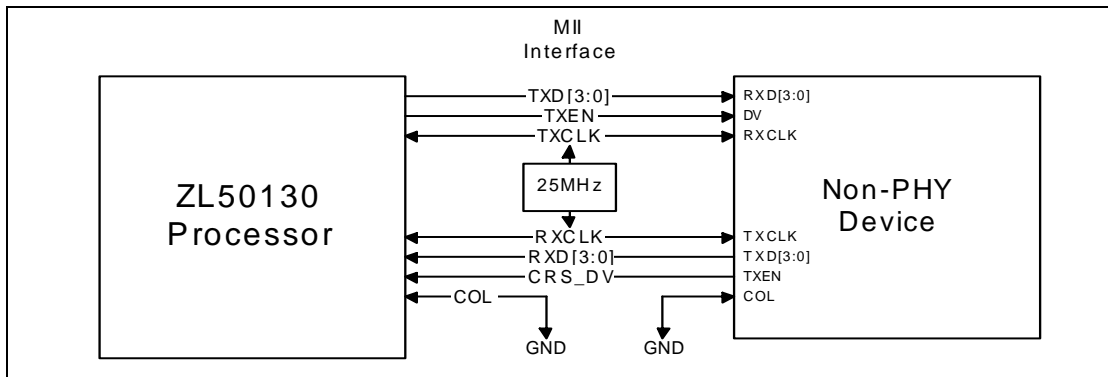


Figure 2 - ZL50130 MII Interface Connections

5.0 Layout Considerations

An important point about MAC-to-MAC connections is with regard to layout of the board. When a common clock is input to both MAC devices, used to sample data by one MAC and drive data by the other MAC, the propagation delay from the clock source must be the same to both MAC devices. As an example, referring to Figure 2, "ZL50130 MII Interface Connections", on page 3, a transmit clock (TXCLK) and a receive clock (RXCLK) is supplied to both MAC devices. For best operation the trace lengths from the TXCLK/RXCLK source to the TXCLK/RXCLK pins on the respective MAC devices should be of equal length. Additionally, it is advantageous to keep the trace lengths as short as possible. When one MAC device drives the clock and data to the other MAC device, as is possible with ZL50405, this issue is of less significance.

6.0 Related Documents

- "ZL50130 Ethernet Pseudo-Wires across a PSN" Data Sheet, Zarlink Semiconductor
- "ZL50130 API User Guide", Zarlink Semiconductor
- "802.3 Local and Metropolitan Networks Part 3: CSMA/CD Access Method and Physical Layer", IEEE, 1995/2000.
- "ZL50405 Managed 5-Port 10/100M Ethernet Switch" Data Sheet, Zarlink Semiconductor
- "Ethernet Switch: MAC-to-MAC Connections" Application Note, Zarlink Semiconductor, ZLAN-30
- "802.3 Local and Metropolitan Networks Part 3: CSMA/CD Access Method and Physical Layer", IEEE, 1995/2000.



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