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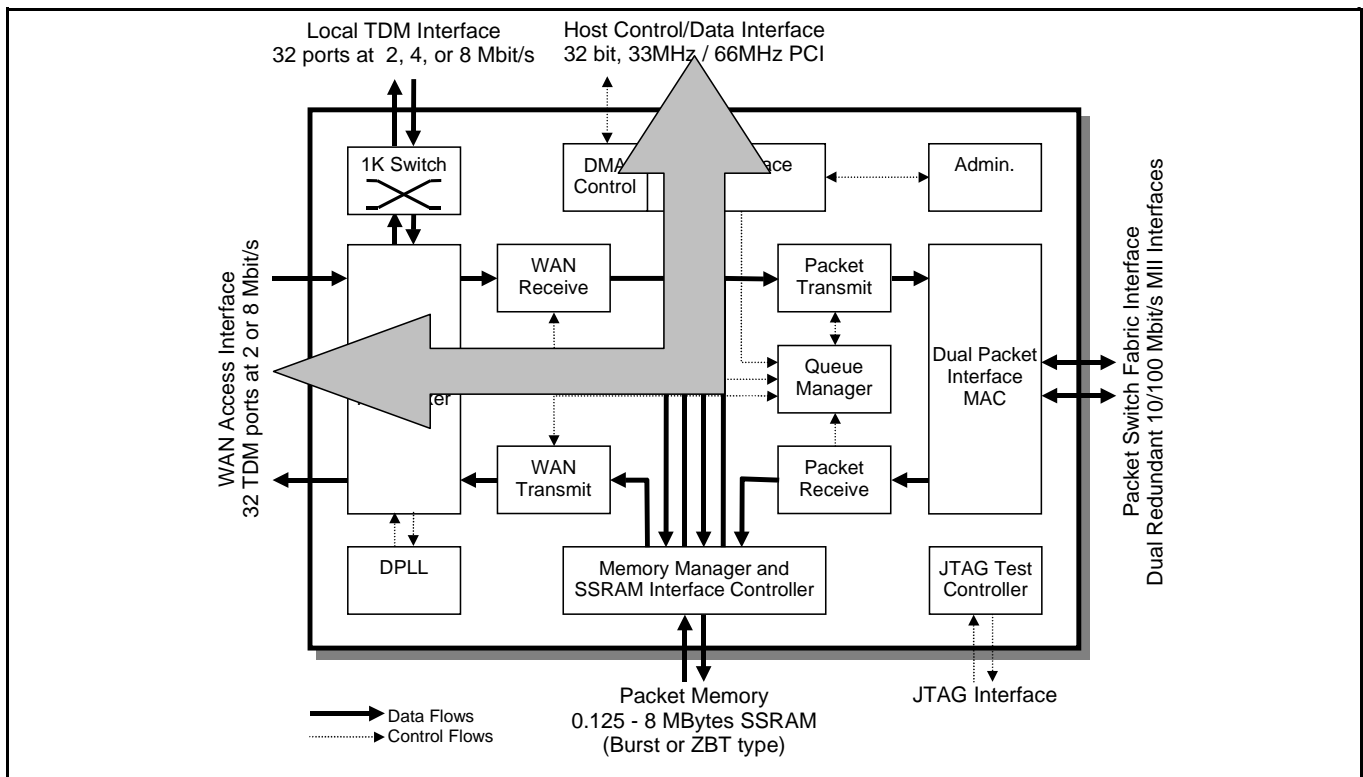
Related Documents

- "MT90880/1/2/3 TDM to Packet Processors" Data Sheet, Zarlink Semiconductor, DS5568, January 2003

1.0 TDM to PCI Bridge

The MT9088x Family may be used to implement a TDM to PCI bridge as shown in Figure 1, "Implementing a TDM-to-PCI Bridge using the MT9088x Family," on page 1. This functionality will allow TDM voice and data to be manipulated by a processor connected to a PCI bus within the system. The MT9088x may be used in this fashion for a variety of applications including voice echo cancellation, ADPCM transcoding, modem handshaking or conference call bridging. The MT9088x may also be used to transfer TDM voice and data over a PCI backplane in the absence of a TDM backplane.

In a typical application using the MT9088x as a TDM to PCI bridge, the TDM interface will carry CBR voice and data, in increments of 64 kbps. The PCI bus will handle packets consisting of CBR voice and data payload with data link, network or transport layer headers, as desired.


Figure 1 - Implementing a TDM-to-PCI Bridge using the MT9088x Family

2.0 Data Path through the MT9088x

The TDM to PCI path is a combination of two paths - the WAN-to-Packet path and the Packet-to-PCI path. These two paths are described in the MT9088x data sheet. Figure 2, "TDM to PCI Data Path," on page 2 shows the data flow for this path. The incoming data from the MT9088x WAN TDM interface is assembled into packets on a frame by frame basis, the CDP/IP/Ethernet headers are appended as appropriate and the Ethernet packet is stored in MT9088x external memory. Subsequently the Ethernet packets are transferred out MII Port A packet interface. At that point the Ethernet packets are looped back via an external pin-to-pin connection between MII Port A and MII Port B. Upon reception at MII Port B the Ethernet packets are sent to MT9088x external memory. From MT9088x external memory the Ethernet packets are then transferred to system memory via DMA transfers on the PCI bus where they may be accessed by the processor.

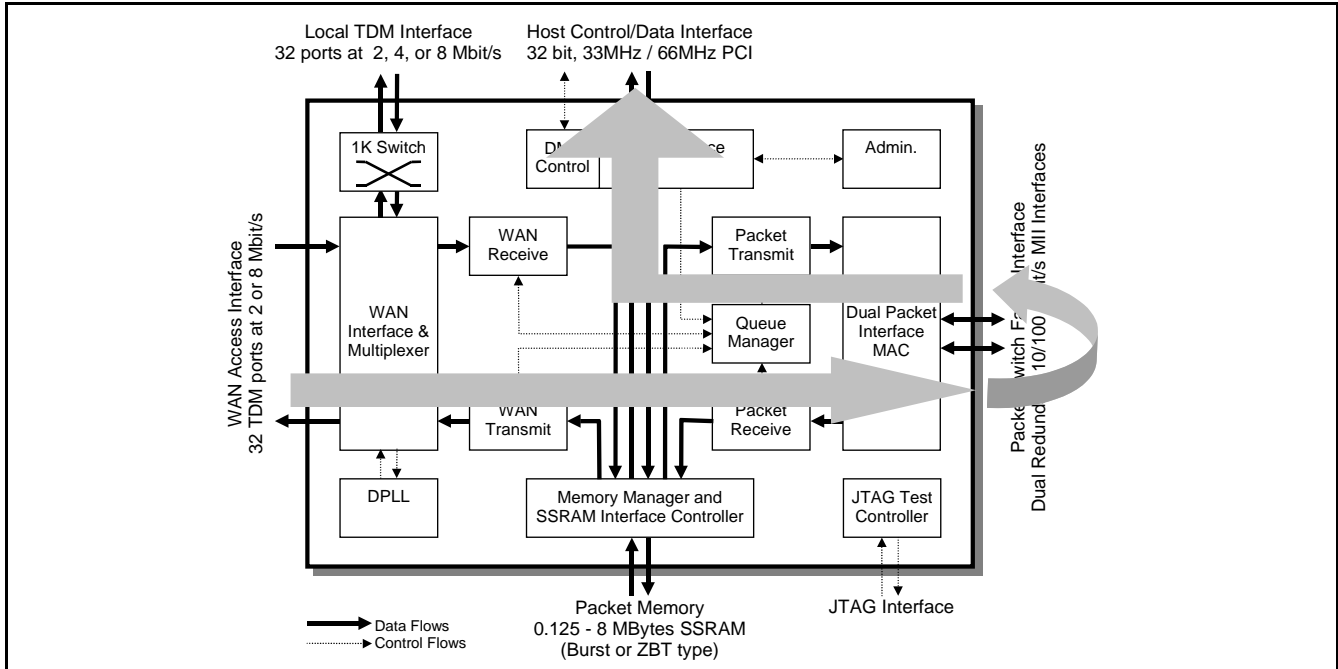


Figure 2 - TDM to PCI Data Path

The PCI to TDM path is also a combination of two paths - the PCI to Packet path and the Packet to WAN path. These two paths are described in the MT9088x data sheet. Figure 3, "PCI to TDM Data Path," on page 3 shows the data flow for this path. The Ethernet packets from the processor are transferred from system memory into MT9088x external memory via DMA transfers on the PCI bus. These Ethernet packets are then sent out MII Port B. At that point the Ethernet packets are looped back to MII Port A via an external pin-to-pin connection between the two MII interfaces. Upon reception at MII Port A the Ethernet packets are written to MT9088x external memory. From there the TDM data is sent out the WAN TDM interface on a frame by frame basis.

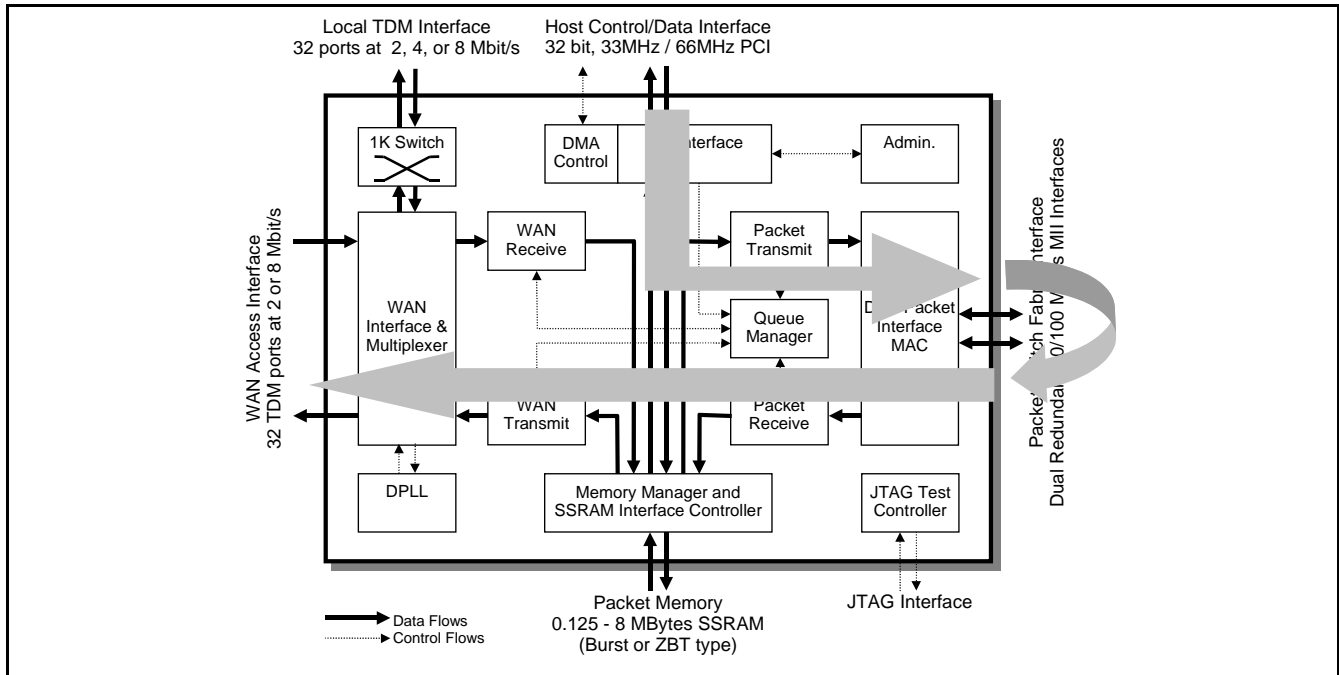


Figure 3 - PCI to TDM Data Path

3.0 TDM Interface Configuration

The WAN TDM interface is based on a 64 kbps (8 bits x 8000 kHz) CBR data rate. The interface consists of either 32 streams running at 2.048 Mbps (32 channels) or 8 streams running at 8.192 Mbps (128 channels). The WAN TDM interface may assume any of the configurations listed in the MT9088x Family data sheet. There is no limitation imposed by this specific application of the MT9088x device.

4.0 PCI Interface Configuration

The PCI interface is compliant with the PCI Revision 2.2 specification. The interface is Master/Target capable, supports a 32-bit bus and runs at 33 MHz. The PCI interface is also capable of operation at 66 MHz, selected through the PCI_M66EN pin. The PCI interface may assume any of the configurations listed in the MT9088x Family data sheet. There is no limitation imposed by this specific application of the MT9088x device.

5.0 Packet Interface Configuration

The packet interface, specifically the MII interfaces Port A and Port B, will be connected externally to each other. The transmit pins of Port A will be connected to the receive pins of Port B. Likewise the transmit pins of Port B will be connected to the receive pins of Port A. Ethernet packets traveling from the TDM interface to the packet interface will be sent out on Port A and will be received on Port B. Ethernet packets traveling from the PCI bus to the packet interface will be sent out Port B and will be received on Port A. The routing in the packet interface will be based on the Context ID value in the Context Descriptor Protocol (CDP) field. It is recommended that the packet interface be configured to operate in 100 Mbps full-duplex mode for this application. Due to the flexibility of the size

and number of connections, a bandwidth calculator spreadsheet is available that will allow for estimating the amount of bandwidth required on the packet interface -- not to exceed 100 Mbps for each uni-directional data flow.

The format of the Ethernet packets, as seen on the packet interface, is shown in Figure 4, "Ethernet Packet," on page 4 below. A typical configuration would likely use only one frame of payload, while the header would contain only the Ethernet header and CDP field.

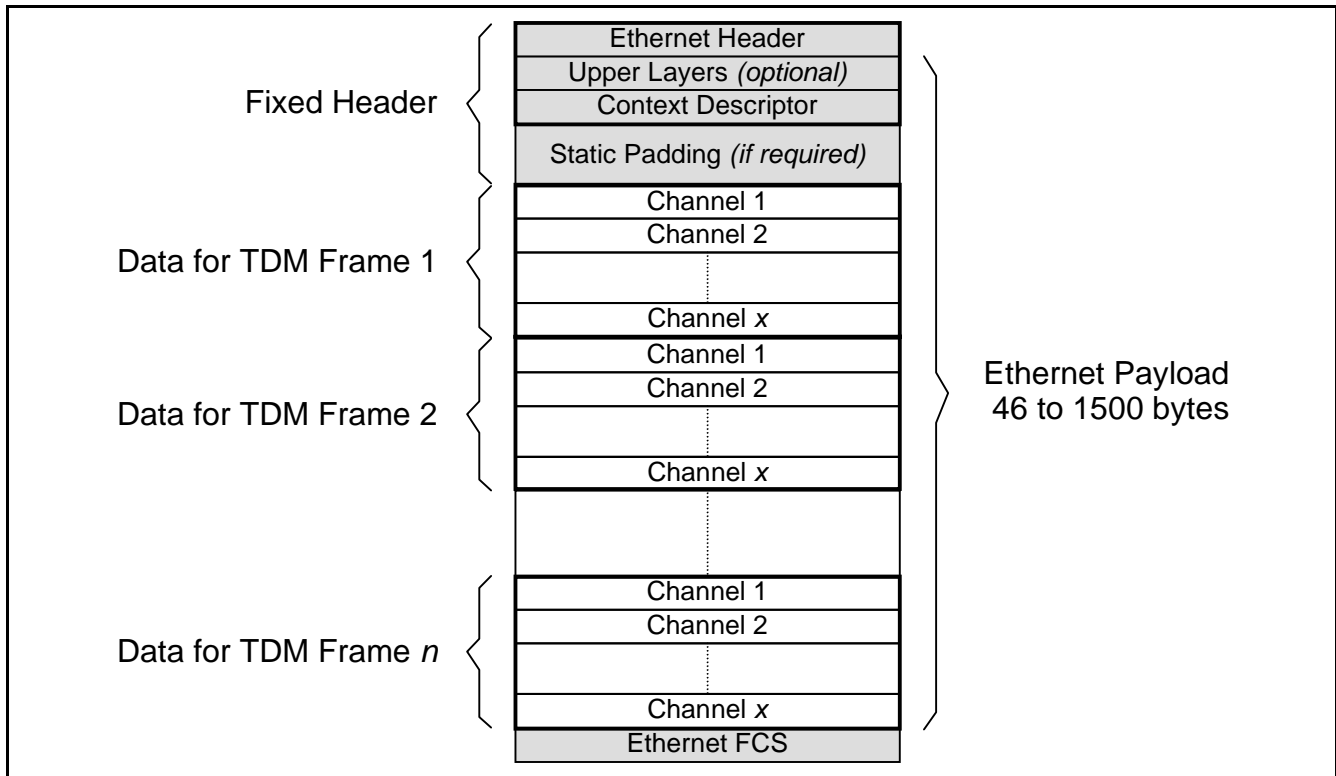


Figure 4 - Ethernet Packet

A table showing the recommended MII pin connections is below. MII Port A interface pins are prefixed by m0, while MII Port B interface pins are prefixed by m1. The MII interface pin-out may be found in the External Interface Description section of the MT9088x data sheet.

Pin Name	Pin #	Connection Pin Name	Connection Pin #	Notes
m_mdc	AF9			No connect
m_mdio	AC10			No connect
m_mint0	AF6			No connect
m0_txd[3:0]	AC8 [3], AF5 [2], AE6 [1], AD7 [0]	m1_rxd[3:0]	AF12 [3], AD13 [2], AE13 [1], AF13 [0]	
m0_txen	AD6	m1_rxdv	AE12	
m0_txclk	AB9			Connect to 25 MHz clock (100 Mbps)
m0_rxd[3:0]	AF8 [3], AE8 [2], AE9 [1], AD9 [0]	m1_txd[3:0]	AC11 [3], AE10 [2], AF10 [1], AD11 [0]	
m0_rxdv	AF7	m1_txen	AD10	

Table 1 - Packet Interface Pin Connections

Pin Name	Pin #	Connection Pin Name	Connection Pin #	Notes
m0_rxclk	AB10			Connect to 25 MHz clock (100 Mbps)
m0_rxer	AD8			No connect
m0_crs	AC9			No connect (full duplex)
m0_col	AE7			No connect (full duplex)
m_mint1	AE11			No connect
m1_txd[3:0]	AC11 [3], AE10 [2], AF10 [1], AD11 [0]	m0_rxd[3:0]	AF8 [3], AE8 [2], AE9 [1], AD9 [0]	
m1_txen	AD10	m0_rxdv	AF7	
m1_txclk	AB12			Connect to 25 MHz clock (100 Mbps)
m1_rxd[3:0]	AF12 [3], AD13 [2], AE13 [1], AF13 [0]	m0_txd[3:0]	AC8 [3], AF5 [2], AE6 [1], AD7 [0]	
m1_rxdv	AE12	m0_txen	AD6	
m1_rxclk	AC13			Connect to 25 MHz clock (100 Mbps)
m1_rxer	AD12			No connect
m1_crs	AC12			No connect (full duplex)
m1_col	AF11			No connect (full duplex)

Table 1 - Packet Interface Pin Connections (continued)

6.0 Memory Interface Considerations

For the TDM to PCI data flow, processor destined Ethernet packets are transferred into system memory by the DMA as they are received on MII Port B. It is expected in this application that the packets that are being transferred to system memory will be accessed on a frequent enough basis by the processor to avoid running out of system memory. Processing packets in system memory on a regular basis will not only limit the latency but will allow for a smaller total system memory size.

For the PCI to TDM data flow, WAN TDM interface destined Ethernet packets are stored in a MT9088x external memory jitter buffer. It is expected in this application that the processor will supply Ethernet packets at a fairly constant rate thereby limiting the need for a large jitter buffer. Once again, due to the flexibility of the size and number of connections, a memory calculator spreadsheet is available that will allow for estimating the amount of external memory required.

The memory interface may assume any of the configurations as listed in the data sheet. However, for cost savings, using the smallest memory for the maximum number and size of connections to be supported would be advantageous. One of the best methods of reducing the size of memory required is to increase the number of frames of TDM data in each packet.

7.0 Conference Bridge Application

By way of example, an application that implements a five participant conference bridge will be discussed in this section. The voice channels of the participants are present on the WAN TDM interface of the MT9088x. The conference bridging/mixing of the channels is performed in a PCI based processor. The data flow may be described as follows. Figure 5, "Conference Bridge Application," on page 6 below shows this application.

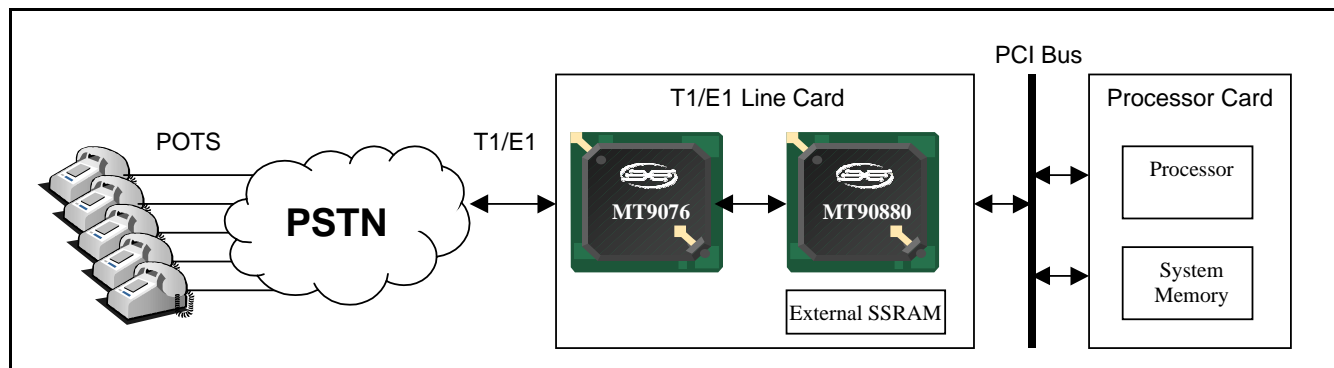


Figure 5 - Conference Bridge Application

The five channels are incoming on the MT9088x WAN TDM interface. Each frame they are sampled and packetized into an Ethernet packet using a specific Context ID - 0x3. This Ethernet packet is sent out MII Port A where it is immediately received on MII Port B due to the external loopback. The Ethernet packet is then routed into MT9088x external memory. At this time the processor is notified that a packet is waiting for transfer. The processor will retrieve this packet from the MT9088x external memory using a DMA transfer over the PCI bus.

The processor will examine the Context ID and determine that this packet contains five channels that require conference mixing. Internal to the processor the five channels will be converted to linear code, mixed and converted back to 8-bit PCM to form five conferenced channels.

The processor will then form a new Ethernet packet with the five conferenced channels using Context ID of 0x3. The processor will transfer this packet by way of a DMA transfer into the MT9088x external memory. From there the MT9088x will send this packet out MII Port B where it will once again be immediately received on MII Port A due to the external loopback. Upon reception, the Ethernet packet will be placed in MT9088x external memory. The five conferenced channels will then be retrieved from MT9088x external memory and sent out the MT9088x TDM interface on the timeslots allocated to Context ID 0x3.

In the above fashion, multiple conference bridges may be implemented simply by changing the Context ID within the Ethernet packet. Additionally different functionality may be supported by the processor, such as echo cancellation and voice compression, selectable based on the Context ID contained in the Ethernet packet.



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