Timing Solutions for Synchronous Telecom Equipment

Maamoun Abou Seido
System Architect
maamoun.seido@zarlink.com
http://timing.zarlink.com

AGENDA

- **Timing solutions for next-generation telecom equipment architectures**
- **AdvancedTCATM(ATCA) synchronization specific requirements**
- **Distributed timing architecture**
- **Centralized timing architecture**
  - Issues in employing multi-stage clock circuitry
  - Achieving clock redundancy while maintaining uninterrupted clock operation during active redundant clock switch-over

NEXT-GENERATION TELECOM EQUIPMENT ARCHITECTURE

- **Competing choices for backplane data bus influences the choice on the employed timing solution**
  - A move towards high-speed TDM backplane to achieve more bandwidth while employing existing equipment architectures
    - *The need for a high-speed TDM clock with low jitter exceeding the physical TDM interface jitter specifications*
  - Several flavors of high-speed serial bus
    - *The need for clocks with ultra-low jitter specifications*
  - IP backplane
    - *Clock distribution only to support line interface requirements*
    - *Advanced technologies to support Timing over Packet*

NEXT-GENERATION TELECOM EQUIPMENT ARCHITECTURE

- **A move towards common telecom platform (trend to open HW architecture) such as AdvancedTCATM (ATCA) architectures lead by:**
  - Pressures on equipment cost
  - System vendors focusing on their core technologies
- **ATCA Synchronization Clock Interface specified to:**
  - Enable applications that require the exchange of synchronous timing information between multiple boards in a shelf, though it does NOT define a time division multiplexed bus
  - Reduce overhead on systems that does not require synchronous clock or have limited requirements

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ATCA SYNCHRONIZATION REQUIREMENTS

- **Six clock buses divided into 3 groups**
  - CLK1 A/B (8kHz, clock or frame pulse),
  - CLK2 A/B (19.44MHz clock), and
  - CLK3 A/B user defined (<100MHz) or Network reference (8kHz, 1.544MHz, 2.048MHz, or 19.44MHz)
- **CLK1 A and B 8kHz shall meet or exceed the requirement of Stratum 4E clock**
- **CLK2 A and B 19.44MHz meet the requirement of Stratum 3 or 3E clock**
- **Each clock is implemented as a differential pair that connects to all slots**
- **The buses are symmetric so that a clock transmitter (master) or receiver (slave) can be located in any slot, shelf manager must manage access to these buses, boards might need to support both transmitter and receiver functions**

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ATCA SYNCHRONIZATION REQUIREMENTS

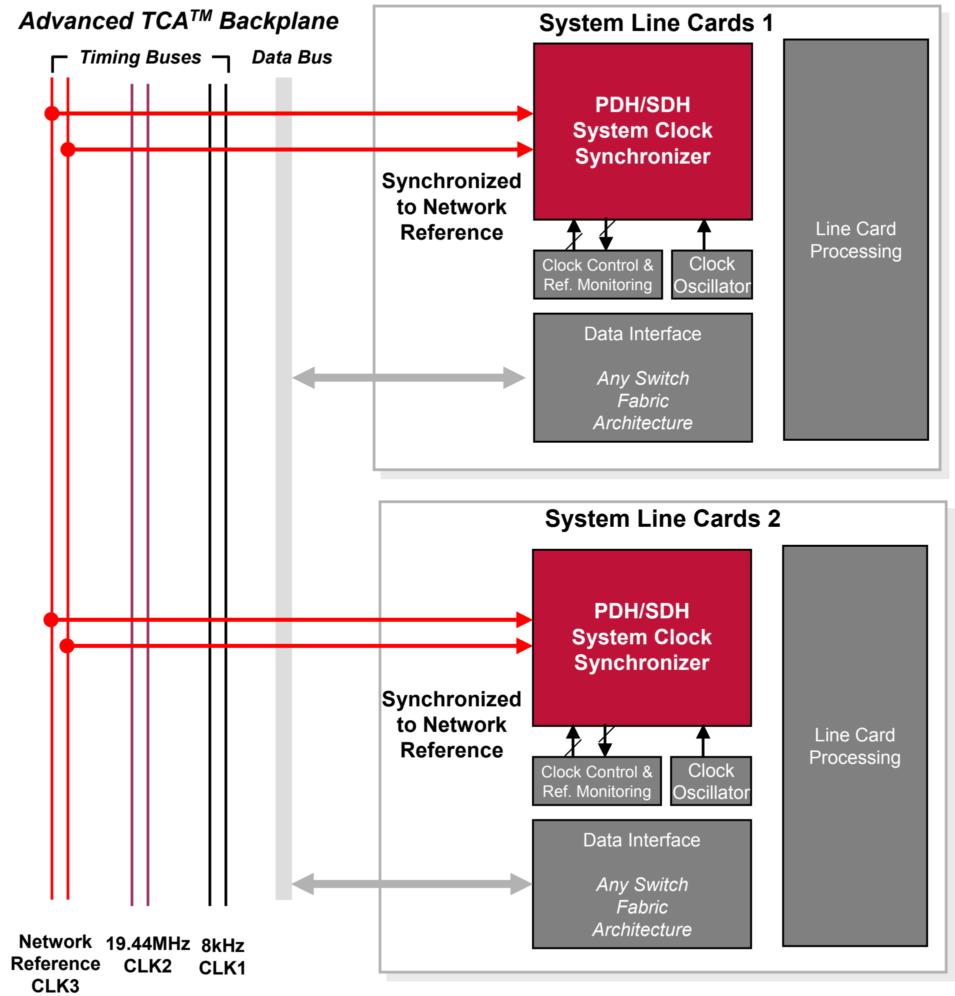
- **Support for two possible timing architectures:**
  - Distributed – Each board would use the network reference to generate its local clocks
  - Centralized – dedicated pair of system clock sources always drive the system clock buses
    - *Frequency and Phase synchronization across the system*
    - *Active and redundant system clock sources that provide edge aligned clock pairs*
    - *Maintain clock quality during active to redundant switch-over*
      - Clock skew between the A and B clocks limited to 10nsec
      - Boards interfacing to clock busses should ride through short duration glitches as defined in Stratum 4E

DISTRIBUTED TIMING ARCHITECTURE

- **Each board receiving external timing could drive the network reference**
- **Board requiring synchronization would use the network reference to generate local clocks**
  - Cards requiring synchronization would have the PLL and the master oscillator to provide network synchronization functions:

    Free-run, holdover, jitter/wander tolerance, transfer and generation and requirements on output phase transients
- **Attractive solution for:**
  - Equipment with limited number of cards requiring synchronization
  - Multi-function box with application that may not require the synchronization overhead (management and cost)

DISTRIBUTED TIMING IN ATCA APPLICATION



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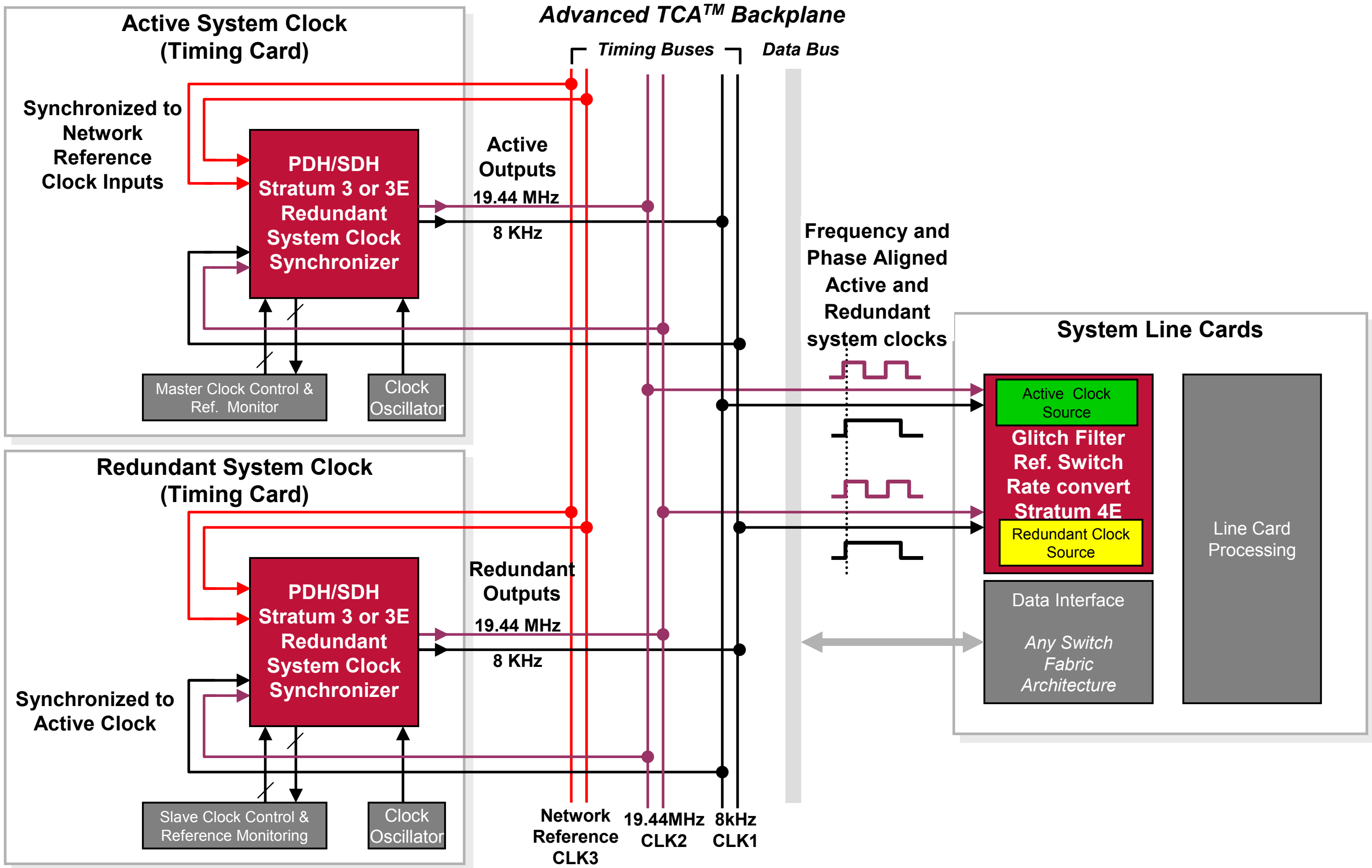
CENTRALIZED TIMING ARCHITECTURE

- **Each board receiving external timing could drive the network reference**
- **Pair of system clock sources always drive the system clock buses**
- **Attractive solution for equipment with more than two cards requiring synchronization**
- **The timing function is distributed between the system clock source and cards requiring the synchronization:**
  - The system clock source would have the PLL and the master oscillator to provide network synchronization functions:

    Free-run, holdover, jitter/wander tolerance, transfer and generation and requirements on output phase transients
  - Cards requiring synchronization would perform:

    Short glitch filtering, hitless reference switching and clock rate conversion and/or jitter filtering

CENTRALIZED TIMING IN ATCA APPLICATION



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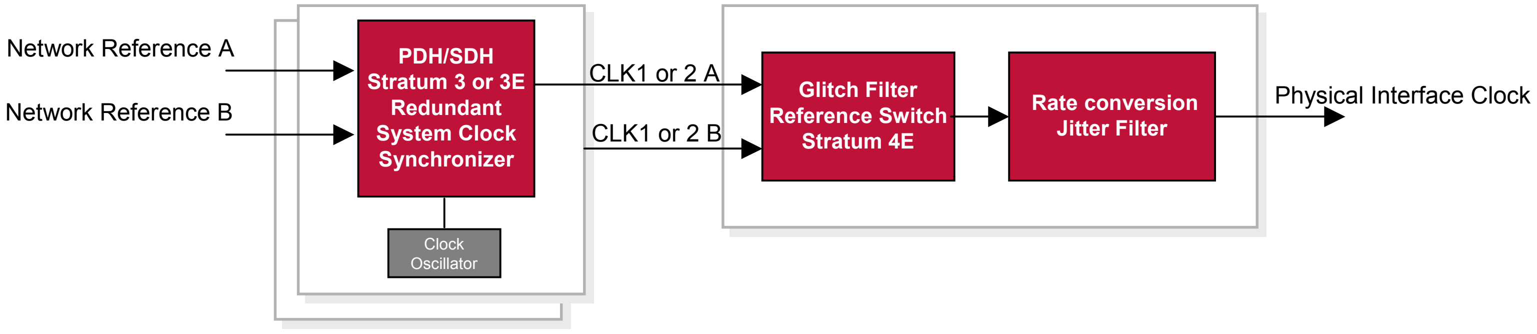
MULTI-STAGE PLL TIMING SOLUTION

- **Entire solution needs to meet physical interface network synchronization requirements**
  - Jitter and wander transfer (corner frequency and peaking) analysis needs to be performed on the entire system
  - Output jitter, wander generation and output phase transient needs to be measured on clock driving the physical interface, not just the clock generated by the system clock source
  - Clock lock time must be measured for the complete clock path, and worst case contributions of different stages need to be considered



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REDUNDANCY WITH TIGHT CLOCK SKEW REQUIREMENTS

- **Active and redundant system clock sources with generating edge aligned clock pairs**
  - System clock circuit in active mode needs to lock to one of the available network references; in redundant mode it needs to track backplane active clock

    Active mode: performs network synchronization functions (free-run, holdover, jitter/wander tolerance, transfer and generation and requirements on output phase transients)

    Redundant mode: allows for tight alignment between input reference and output clock, even in the presence of expected level of network jitter and wander
  - System clock circuit switch-over from redundant to active modes of operation need to be transparent

    The redundant board clock circuitry should track the active clock reference with minimal input to output phase error, or

    The redundant board output clocks and frame pulses could be phase adjusted to compensate of any known PCB routing delays between the active and the redundant clocks

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