

Contents

AN5791

Issue 1

August 2002

1.0 Introduction**2.0 Application Scope****3.0 Emulating the TDM Backplane****4.0 Full Cross-Connect****5.0 Guaranteed Traffic Transmission****5.1 MT90880 Ingress Configuration****5.1.1 MT90880 LAN Queue Depth****5.2 Ethernet Switch Configuration****5.2.1 MVTX2604 Input Buffer Depth****5.3 MT90880 Egress Configuration****1.0 Introduction**

The MT90880 device is a highly flexible TDM to Packet network access processor incorporating a TDM switch, and Dual 100Mbit MACs. There are four device versions; this application note references only the 1K channel device, but all devices could be used in the same manner. The full range of devices is as follows:

- MT90880 1K channels with 1K channel non-blocking TDM switch and Dual 100Mbit MACs
- MT90881 1K channels with Dual 100Mbit MACs
- MT90882 256 channels with 256 channel non-blocking TDM switch and Dual 100Mbit MACs
- MT90883 256 channels with Dual 100Mbit MACs

2.0 Application Scope

When combined with Zarlink's Ethernet Switches, the MT90880 can be used to replace the TDM backplane infrastructure in conventional Telecommunication systems with a packet backplane. The advantages of using a packet medium for transport of TDM services include:

Scalability

As Access System densities increase from 1k channels to OC3 and beyond, scaling of the system architecture is a crucial factor in keeping costs to a minimum.

Efficiency

TDM equipment dedicates capacity to all channels, whether in use or not. Use of a packet-based system allows the available bandwidth to be statistically multiplexed, taking advantage of the fact that not all channels are active all the time.

Service provisioning

It is easier to add new services by adding new line input cards or resource cards. These are not constrained to be in the same physical rack, as with a TDM backplane system.

Cost

Network hardware is readily available at lower cost than equivalent TDM equipment, reducing the overall cost of ownership.

Physical distribution

Equipment may be physically distributed over a wider area, connected either by simple twisted pair network cable, or by fibre. This allows the footprint for co-located equipment (for example) to be small, with the main resources located elsewhere on the network.

A TDM backplane must align high-speed data and clocks, which limits the physical size of the backplane to a single rack.

This type of structure can be used in applications as diverse as multi-service access platforms and voice over IP gateways. Figure 1 shows a multi-service access platform based on an Ethernet backplane using the MT90880.

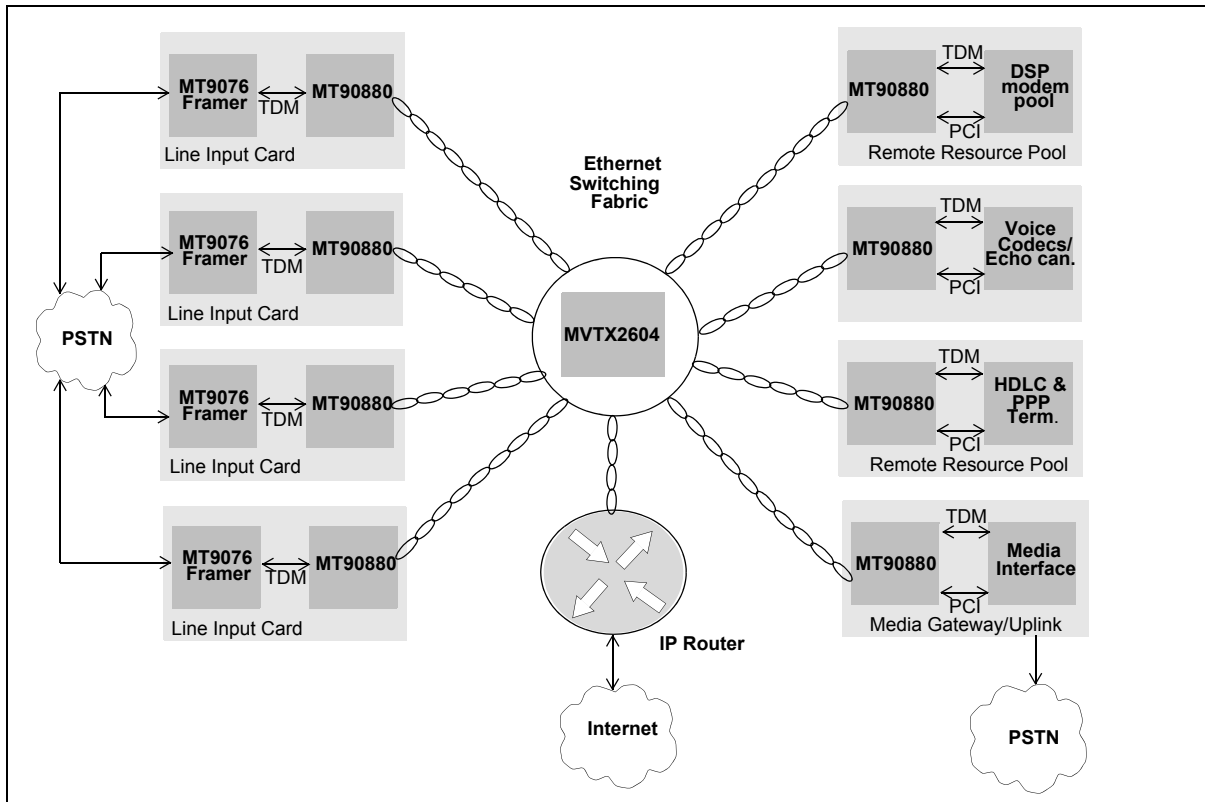


Figure 1 - Multi-service Access Platform using the MT90880

3.0 Emulating the TDM Backplane

If packet based backplanes are to replace TDM backplanes, they must exhibit the same characteristics, particularly when dealing with voice:

1. Cross-connect any TDM channel with any other.
2. Reliable transmission of all traffic. (No missing bytes and all the bytes in the correct order)
3. Low latency data transfer, critical for voice traffic.
4. Provision of an accurate backplane clock, available to all linecards.

4.0 Full Cross-Connect

The MT90880 allows any TDM channel from any TDM stream to be joined together into a flow of packets (or context). The context can be routed across the packet network to any destination. The combination of MT90880 and packet network allows a full cross-connect function to be realised.

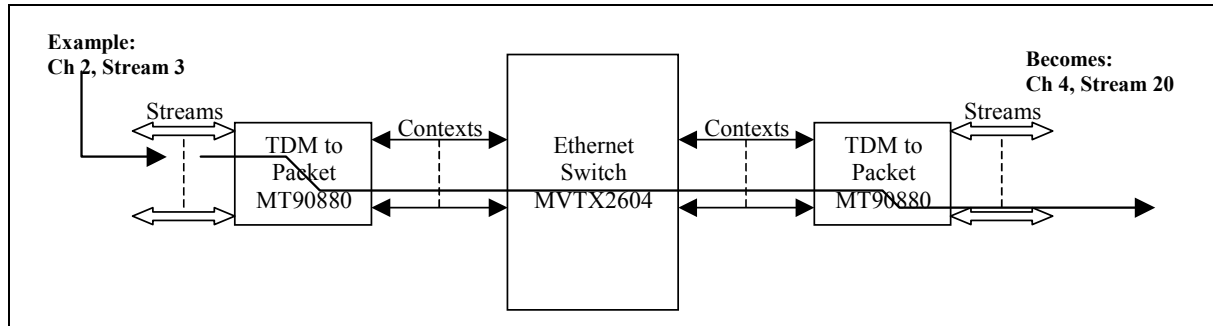


Figure 2 - Full Cross-Connect Function

5.0 Reliable Traffic Transmission

To achieve reliable transmission of TDM traffic over a packet backplane the backplane must be configured so packets are not delayed, lost, corrupted or reordered. This can be achieved, provided each element of the packet network is provisioned with sufficient bandwidth and buffer capacity. Figure 3 below shows a simple packet network for the transmission of TDM traffic.

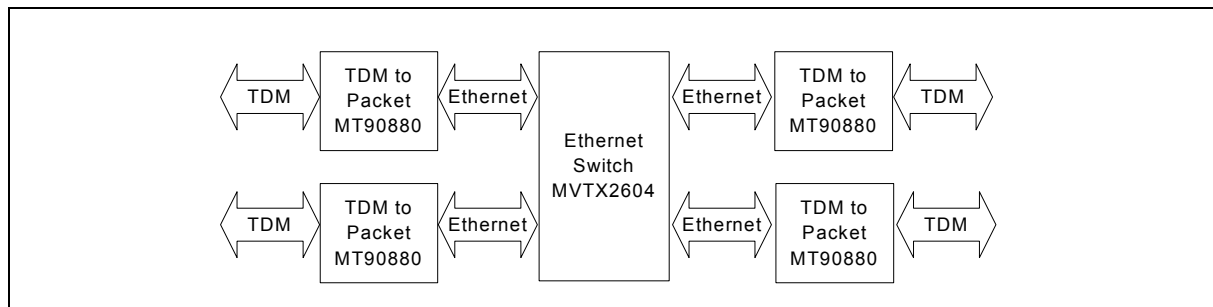


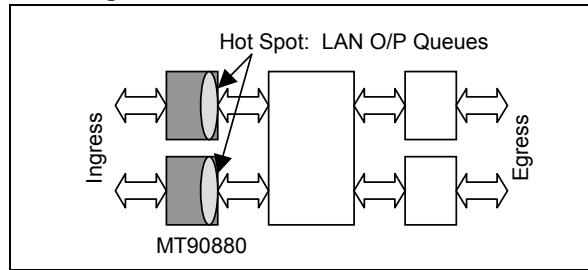
Figure 3 - TDM transmission over a switch packet network

The MT90880 device automatically builds a "jitter buffer" in the queue of packets awaiting transmission on the TDM bus, which encompasses the PDV present in the network. If the network has a large PDV the device will translate this into a large jitter buffer, up to the maximum TDM queue depth increasing the total latency. Therefore it is important to minimise both delay and delay variation in the packet network to maintain low latency TDM data communication.

If the guidelines in this application note cannot always be followed and the network becomes temporarily overloaded with too much TDM traffic for the available bandwidth, (e.g. the control CPU allocates too much traffic to an Ethernet link), then it is not possible to deliver all the data and to achieve low latency. For voice traffic low latency is very important. To achieve low latency it is better to discard late packets, as if they are buffered and delivered late they will increase the network PDV. In response to the late packets the destination MT90880 will build a jitter buffer to match the increased network PDV and thereby increase the TDM data latency up to the maximum TDM queue depth for all future packets.

The following sections specify how to achieve reliable packet transmission using Zarlink's MT90880 and Ethernet Switching products.

5.1 MT90880 Ingress Configuration



On the Ingress side of a Packet Backplane network, the appropriate number of MT90880 devices must be configured to handle the number of TDM streams entering the system. Each MT90880 can handle a maximum of 1024 channels. It is important to ensure a backlog of packets does not build up in the LAN output queues of the MT90880 devices. To achieve this, each device must be configured as follows:

1. The TDM data must be routed to a specific output queue on each LAN port. Non TDM data must use a different queue.
2. The TDM packet queues must be allocated a guaranteed slice of the Ethernet bandwidth. The MT90880 supports packet scheduling onto the Ethernet links using strict priority or weighted fair queuing (WFQ). If strict priority is used then the TDM packets must be allocated the highest priority. If WFQ is used then the TDM packets must be allocated sufficient bandwidth to handle the maximum loading.
3. The control CPU must balance the routing of TDM packets between the two Ethernet ports on each MT90880 device, thus ensuring neither of the links is loaded beyond the bandwidth allocated to TDM packets.
4. The buffer thresholds for the TDM packet output queues must be allocated sufficient space to hold a short-term build up of TDM packets while queued before transmission.
5. Do not provision buffer space above the minimum requirement for the TDM packet queues.

Large output buffers allow a backlog of packets to build up if a problem occurs on the network. When the network problem is removed the packet backlog will be delivered to the destination MT90880 as late packets increasing the network PDV. The destination MT90880 device will build a larger jitter buffer, up to the maximum TDM queue depth, encompassing the increased PDV. The change in jitter buffer increases the system latency.

If a small output buffer is used then packets are discarded if a network problem occurs instead of being delivered as late packets. As a result the destination MT90880 device does not see an increased PDV and maintains a small system latency. The lost packets will reduce the jitter buffer in the destination MT90880 but this will be quickly rebuilt when the network problem is removed.

6. The overall threshold for all LAN queues must be greater than the sum of the thresholds for the individual queues. This ensures that packet overload on a non TDM queue cannot result in TDM packets being discarded if the overall LAN threshold is exceeded.
7. Set the appropriate bits in the header for the TDM data packets so the network gives them a high priority. (e.g. VLAN priority, IP TOS)

5.1.1 MT90880 LAN Queue Depth

The following table shows the queue depth required, guaranteeing smooth operation of the MT90880 for various traffic assumptions.

Traffic assumptions	1	2	3	4	5
Number of TDM channels (A)	1024	1024	1024	1024	1024
Number of contexts (B)	16	32	64	128	16
Number of channels per context (A/B)	64	32	16	8	64
TDM frames per packet	1	1	2	4	4
TDM data bytes per packet	64	32	32	32	256
Header size	20	20	20	20	20
Packet Size (bytes)	84	64	64	64	276
MT90880 Requirements					
Ethernet bandwidth used (Mbits/s)	110	180	180	180	76
LAN output buffer depth required (packets) <i>Required for each LAN output queue.</i>	8	16	32	64	8
Allowance for large 1500 byte packet (packets)	8	16	16	16	2
Total output buffer depth (packets) <i>Required for each LAN output queue.</i>	16	32	48	80	10
Total output buffer depth (granules)	16	32	48	80	30
Total size (kbytes)	1.8	3.5	5.3	8.8	3.3

Table 1 - MT90880 LAN Queue Depth

Description of calculations for column 2 above

Assume each MT90880 device supports 1024 channels divided between 32 contexts each with 32 channels and a packet is formed for each context every TDM frame period. Assuming a 20byte packet header, each packet will be 52 bytes long. To conform to the minimum Ethernet packet size the packet must be padded up to 64bytes. With a 12 byte inter packet gap plus 8 byte preamble plus 4 byte FCS the TDM packets will consume 180Mb/s of the Ethernet bandwidth. This is below the available 200Mb/s leaving some spare capacity for control and signalling packets.

The above example will generate 32 packets every frame period. For the MT90880 family, external memory is divided into 'granules', which equate to 112bytes and each packet, will occupy just one granule. The TDM traffic is split between the two LAN ports and 16 granules must be allocated to the queue on each port. An extra 32 granules are required to allow for the case where the packets are held up while transmission of a large (1500 byte) packet is completed. Therefore a total buffer depth of 48 granules must be provided for each LAN queue for TDM packets.

5.2 Ethernet Switch Configuration

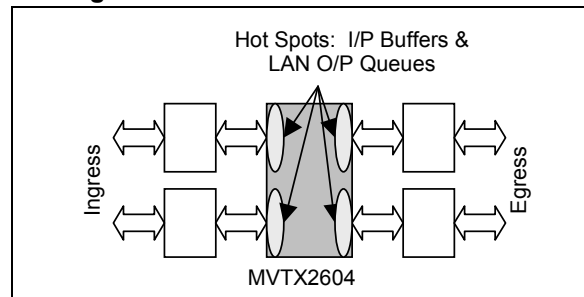


Figure 4 below shows a simplified block diagram for an Ethernet Switch. Packets arrive on the MII Ethernet connections and are stored in the input buffers. Each packet is classified to determine the destination port and then a pointer for the packet is placed in the relevant output queue.

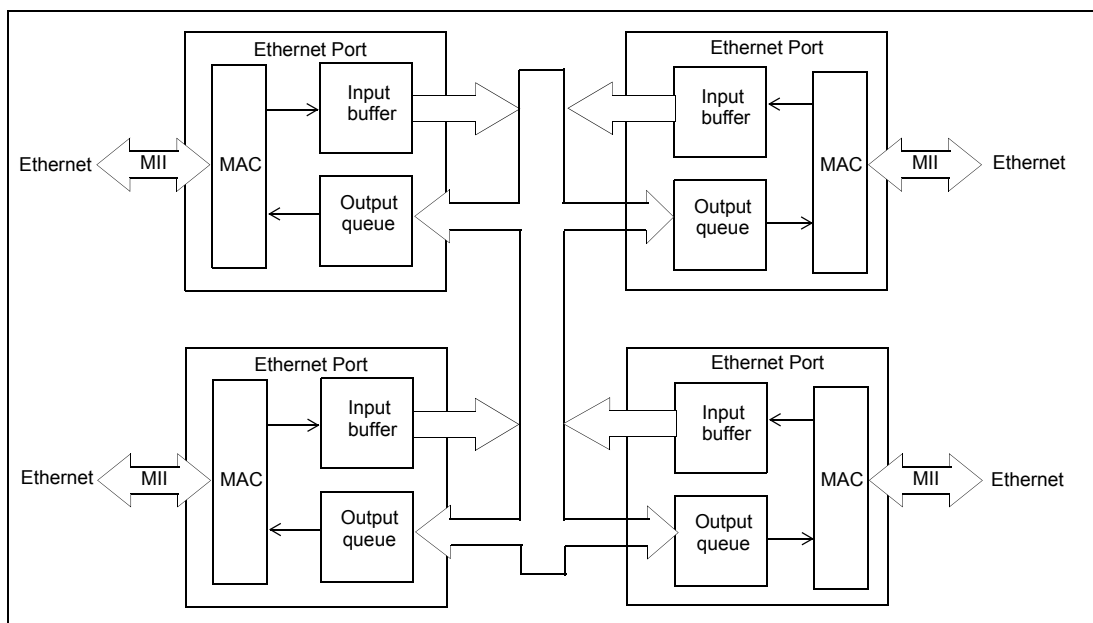


Figure 4 - Simplified Ethernet Switch Block Diagram

For reliable operation in a TDM replacement Ethernet backplane application the switch must be configured so that it never loses TDM packets as follows:

1. The TDM data must be routed to a specific output queue on each switch port. Non TDM data must use a different queue.
2. The TDM traffic packet queues must be allocated a guaranteed slice of the Ethernet bandwidth. The MVTX2604 supports packet scheduling using strict priority or weighted fair queuing (WFQ). If strict priority is used then the TDM packets must be allocated the highest priority. If WFQ is used then the TDM packets must be allocated sufficient bandwidth to handle the maximum loading.
3. The control CPU must balance the routing of TDM packets between the two Ethernet ports destined for a single MT90880 device ensuring neither of the links is loaded beyond bandwidth allocated to TDM packets.
4. Configure the Ethernet switch to recognize TDM packets so they can be scheduled at a high priority. The MVTX2604 switch device supports packet classification using:
 - VLAN Priority field.
 - DS/TOS field in an IP packet.
 - UDP/TCP logical ports.
 - Port based priority

5. The buffer thresholds for the TDM packet output queues must be allocated sufficient space to hold a short-term build up of TDM packets before transmission.
6. Do not provision buffer space above the minimum requirement for the TDM packet queues.

5.2.1 MVTX2604 Input Buffer Depth

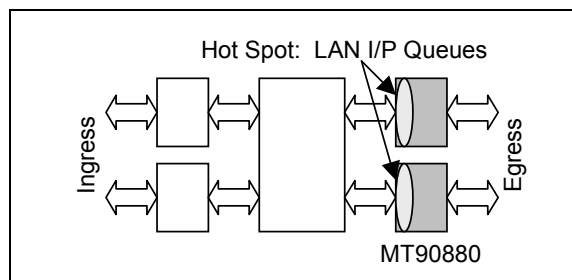
To guarantee no packets are lost when being routed by the Zarlink MVTX2604 managed switch, the Input Buffer depth must be set correctly. The table below shows the depth of buffer required.

Traffic assumptions	1	2	3	4	5
Number of TDM channels (A)	1024	1024	1024	1024	1024
Number of contexts (B)	16	32	64	128	16
Number of channels per context (A/B)	64	32	16	8	64
TDM frames per packet	1	1	2	4	4
TDM data bytes per packet	64	32	32	32	256
Header size	20	20	20	20	20
Packet Size (bytes)	84	64	64	64	276
Ethernet Switch Requirements					
Ethernet bandwidth used (Mbits/s)	110	180	180	180	76
LAN output buffer depth required (packets)	16	32	64	128	16
Allowance for large 1500 byte packet	16	32	32	32	4
Total output buffer depth (packets) For each LAN queue.	24	48	64	96	12

Table 2- Ethernet Switch Input Buffer Depth

The example conditions are the same as described above in the MT90880 section. The main difference is that the MVTX2604 allocates its buffer storage in units of complete packets instead of granules.

5.3 MT90880 Egress Configuration



A "jitter buffer" of packets must be stored in the external memory to allow for the network packet delay variation (PDV). PDV calculations are shown in section 6. The MT90880 can be configured to wait for a number of TDM frame periods after the first packet has arrived before commencing transmission. The delay starting transmission allows a number of packets (or jitter buffer) to build up in the TDM output queues.

For low latency applications it is recommended that the MT90880 jitter buffer delay is disabled and TDM transmission is started as soon as the first packet arrives. When a packet arrives late, due to the network PDV, the MT90880 will send underrun data for a number of TDM frames periods required to fill the gap. When the packet finally arrives it will be sent. This effectively increases the jitter buffer delay by the amount of time the packet was late. Over a period of time as packets experience the full network PDV a jitter buffer of the required size will be built in the output queue. Provided the packet network PDV remains stable no further underruns will occur.

The MT90880 device must be configured to limit the jitter buffer depth by setting the maximum TDM queue depth. In packet backplane mode the MT9088x device can be configured to store between 0 and 15 packets. The TDM queue depth must be set to the expected packet PDV in frame periods, see Table 3 Example Latency Calculations.

6.0 Calculation of End to End Latency

Figure 5 below shows the delays experienced by the TDM traffic as it passes across the packet backplane, all other latencies incurred by each of the devices on the path, are insignificant compared to those shown.

- "Packet formation delay". This will depend on the number of TDM frames the device has been instructed to include in each packet. If 4 frames are included the delay will be $4 * 125 = 500\mu s$.
- "Packet transmit delay" - Once packet formation is complete the packets are placed in a queue ready for transmission over the network.
- "Packet Switch delay" - Packets arriving at the switch will be queued, using the input buffers, ready for transmission to the destination device.
- "Jitter buffer" - The destination MT90880 holds the packets in a queue (held in external memory) ready for transmission as TDM data. Some of the jitter buffer is held in the WAN Tx, which has five sixteen byte internal buffers.

Selecting the number of TDM frames of data to be place in each packet directly controls the "Packet formation delay". The number of active channels and the number of active contexts indirectly affect the other delays.

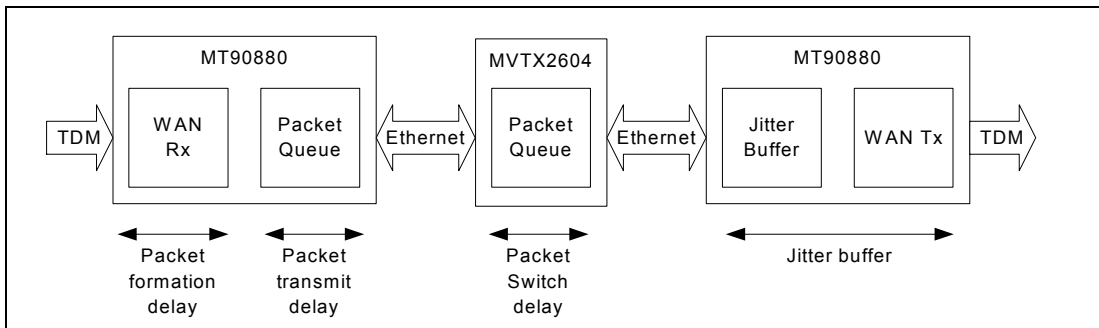


Figure 5 - TDM Latency using packet backplane

Table 3 below shows calculations of backplane latency for 5 traffic assumptions.

Traffic assumptions	1	2	3	4	5
Number of TDM channels (A)	1024	1024	1024	1024	1024
Number of contexts (B)	16	32	64	128	16
Number of channels per context (A/B)	64	32	16	8	64
TDM frames per packet	1	1	2	4	4
TDM data bytes per packet	64	32	32	32	256
Header size	20	20	20	20	20
Packet Size (bytes)	84	64	64	64	276
TDM Latency Calculations (μs)					
Packet Formation delay	125	125	250	500	500
Packet Transmit Delay					
Minimum Packet transmit delay	9	7	7	7	24
Large packet delay	122	122	122	122	122
Maximum Packet transmit delay	191	235	347	573	314
Packet Switch delay					
Minimum Packet Switch delay	9	7	7	7	24
Large packet delay	122	122	122	122	122
Maximum Packet Switch delay	191	235	347	573	314
Packet PDV	364	456	680	1132	580
Packet PDV (Frame Periods)	3	4	5	9	5
TOTAL maximum delay (μs)	625	625	1000	1750	1250
TOTAL maximum delay (Frame Periods)	5	5	8	14	10

Table 3- Example Latency Calculations

For the example in column 2 above, a new packet is formed each TDM frame period, so the "packet formation" delay is 125 μ s. Each TDM packet is 64 bytes, which will take 7.04 μ s to transmit across the LAN at 100Mbit/s. If we assume a worst case where the packet is queued behind all the other TDM traffic packets plus a large 1500 byte packet from a different queue, for example the CPU, then it could take a maximum of 235 μ s before transmission is complete.

Within the Ethernet Switch the same calculations apply for the transmission onto the destination MT90880 device, because the classification and routing of the packets is insignificant when compared to the transmission delay.

The packet delay variation (PDV) will be the difference between the transmission times in the queues in the source MT90880 and the Ethernet Switch. $(235-7)*2 = 456\mu$ s. The PDV would be reduced by 244 μ s if the packet size is restricted and 1500 byte packets do not occur.

The total maximum delay is the sum of the Packet Formation Delay, the Packet Transmit Delay and the Packet Switch Delay, this equates to at 625µs (rounded from 595µs) or 5 TDM frame periods. The delay is rounded up to the nearest frame period because the TDM output always commences at the start of a frame.

7.0 TDM clock provision across the network

There are a number of possible solutions for the provisioning of an accurate TDM clock across the packet network.

1. Route an 8 kHz frame pulse to each line card from a central source and use the MT90880 DPLL to generate the local TDM clock.
2. Route TDM clock and frame pulse signals to each line card from a central source.
3. Another alternative is to transmit the clock across the packet network. This technique is the subject of a separate application note.

The following table reviews the clocking differences between and TDM and packet based backplane.

TDM backplane	Packet backplane
Single clock and framepulse used along the backplane.	The same clock frequency must be used for ingress and egress of TDM data.
High-speed clock (up to 32Mbits/s) must be used for high bandwidth applications.	High-speed TDM clock need not be used to achieve a large system.
Accurate clock and data phase alignment very important for correct data transmission.	Clock alignment less important between TDM nodes. Clock and data alignment required at each TDM node. This is easier to achieve using 2 or 8Mbits/s data rates.
A TDM backplane restricted to a single rack.	A packet based backplane can be distributed between racks over a wide area.

Table 4- Comparison of TDM and packet based backplane clocking

8.0 Glossary

- CPU - Central Processing Unit
- FCS - Frame Check Sequence
- LAN - Local Area Network
- PDV - Packet Delay Variation
- PLL - Phase Locked Loop
- TDM - Time Division Multiplexing
- WAN - Wide Area Network
- WFQ - Weighted Fair Queuing



**For more information about all Zarlink products
visit our Web Site at
www.zarlink.com**

Information relating to products and services furnished herein by Zarlink Semiconductor Inc. or its subsidiaries (collectively "Zarlink") is believed to be reliable. However, Zarlink assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service or for any infringement of patents or other intellectual property rights owned by third parties which may result from such application or use. Neither the supply of such information or purchase of product or service conveys any license, either express or implied, under patents or other intellectual property rights owned by Zarlink or licensed from third parties by Zarlink, whatsoever. Purchasers of products are also hereby notified that the use of product in certain ways or in combination with Zarlink, or non-Zarlink furnished goods or services may infringe patents or other intellectual property rights owned by Zarlink.

This publication is issued to provide information only and (unless agreed by Zarlink in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. The products, their specifications, services and other information appearing in this publication are subject to change by Zarlink without notice. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. Manufacturing does not necessarily include testing of all functions or parameters. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to Zarlink's conditions of sale which are available on request.

Purchase of Zarlink's I²C components conveys a licence under the Philips I²C Patent rights to use these components in and I²C System, provided that the system conforms to the I²C Standard Specification as defined by Philips.

Zarlink, ZL and the Zarlink Semiconductor logo are trademarks of Zarlink Semiconductor Inc.

Copyright Zarlink Semiconductor Inc. All Rights Reserved.

TECHNICAL DOCUMENTATION - NOT FOR RESALE
