Zarlink Medical RF, SiP and the Future

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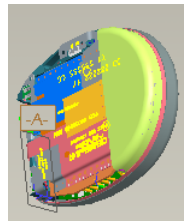
Zarlink Semiconductor

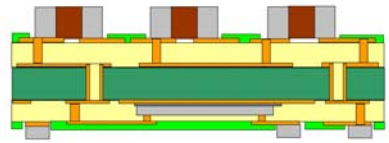
NMI at TWI, 12 Dec 07

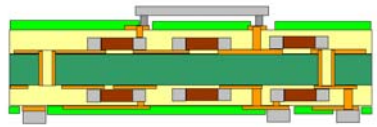
ZARLINK SEMICONDUCTOR

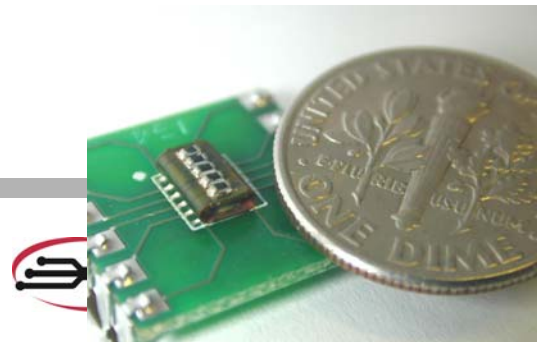
Introduction

- **Introduction to the Packaging Foundry at Zarlink**
- **Design requirements for RF SiP in Pacemakers**
- **Zarlink's embedded component research projects**
- **Review of other embedded component design options**
- **The future of embedded component in Zarlink RF SiP's**









Introduction to Zarlink Microelectronic's Packaging Foundry

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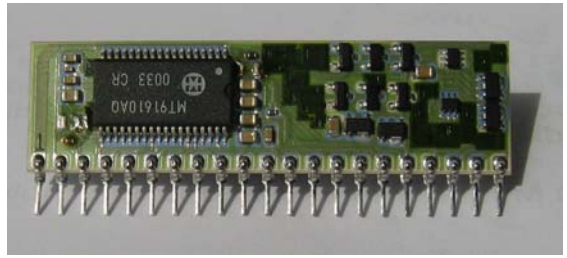
CONFIDENTIAL

Zarlink Microelectronics

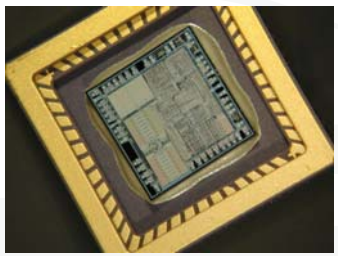
- **Packaging foundry**
  - 75% packages for implantable medical devices
  - 25% merchant subcontract packaging
- **Module and Packaging design**
- **75 employees**
- **Based in Caldicot, South Wales**
- **Part of a multinational company – Zarlink Semiconductor**

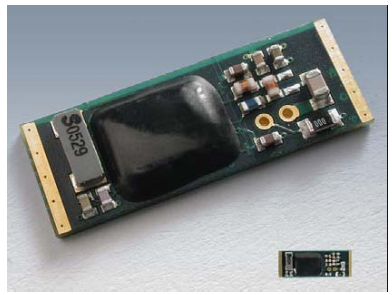
History



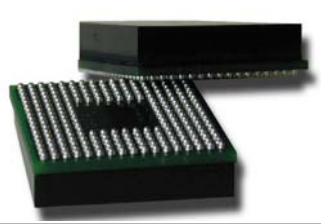
- **1983 Established as manufacturer of ceramic hybrid circuits**
  - SLIC for telecom applications

- **2001 Packaging facility**





- **Specialist packaging**
- **Mainly Medical Microelectronics**



Design requirements for the Pacemaker

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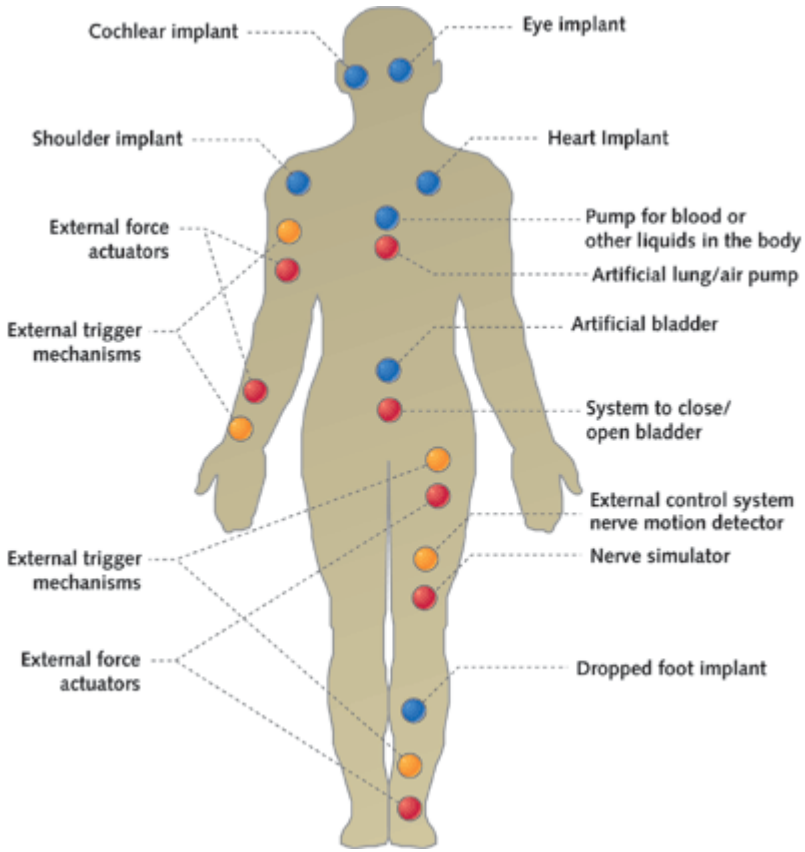
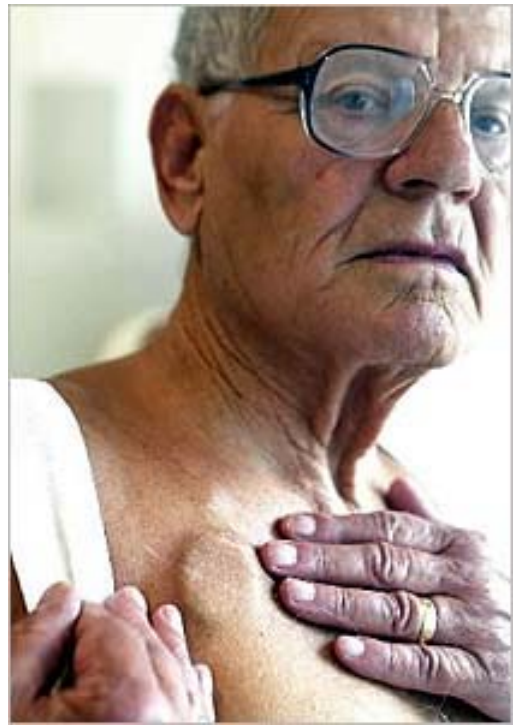
Examples Diseases and Implants

- Implantable electronic devices treat these conditions:
  - **Profound Deafness**
    Cochlear Implant
  - **Heart conditions**
    Pacemakers
  - **Diabetes**
    Insulin pumps
  - **Paralysis**
    Stroke victims
    “Dropped Foot Implant”



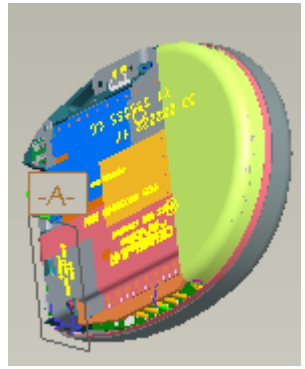
Pacemakers

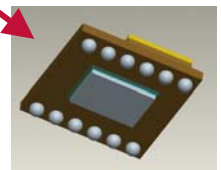
- **Pacemakers dominate the implant market**
- **It is the most effective was to treat arrythmia**
- **Relatively young people affected by arrythmia**
- **Arrythmia is a common condition**
- **Most other implant devices:**
  - Too expensive or risky
  - Only the elderly affected
  - Rare condition, low volume

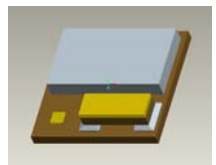


Pacemaker requirements for new RF SiP design technologies

- **Space is a premium**
- **SiP format**
  - Narrow long PCB circuits
  - Low profile SMT format
- **Reliability**
- **Provide RF shielding?**
- **Component protection - handling**
- **Reduced cost**







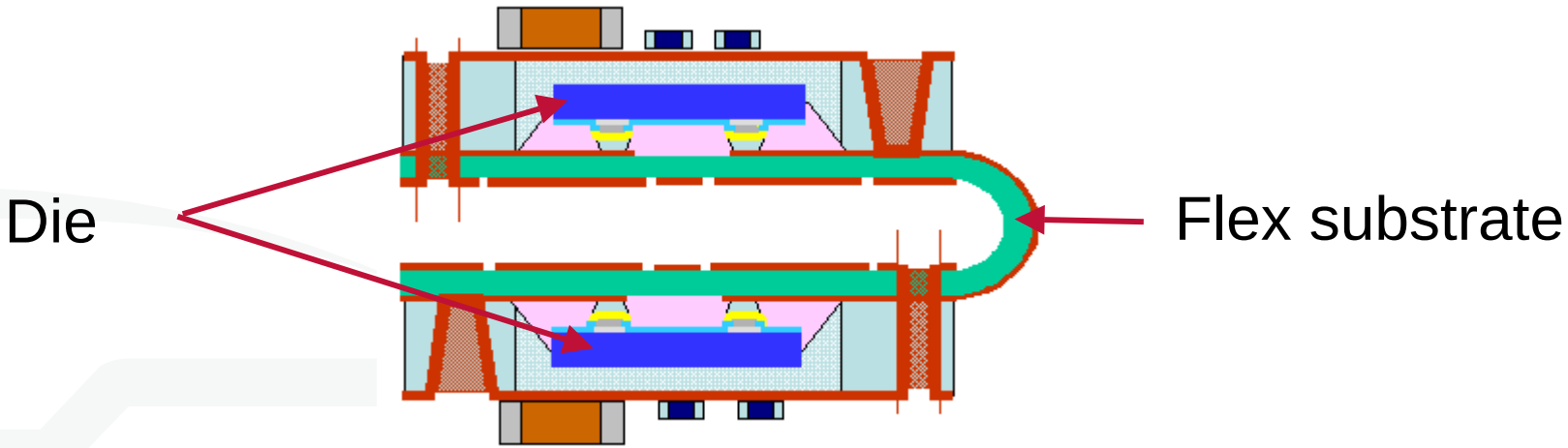
Zarlink research projects

- **SHIFT**
  - Active die embedded in flex
  - EU FP6 integrated project, 1st demonstrator due shortly
- **CiP**
  - Embedded die in PCB
  - Zarlink funded project
  - Collaboration with Technical University of Berlin
- **ADEPT**
  - Embedded passive components
  - Emphasis on characterisation and simulation
  - Collaboration with TWI

SHIFT project concept

Objectives of SHIFT

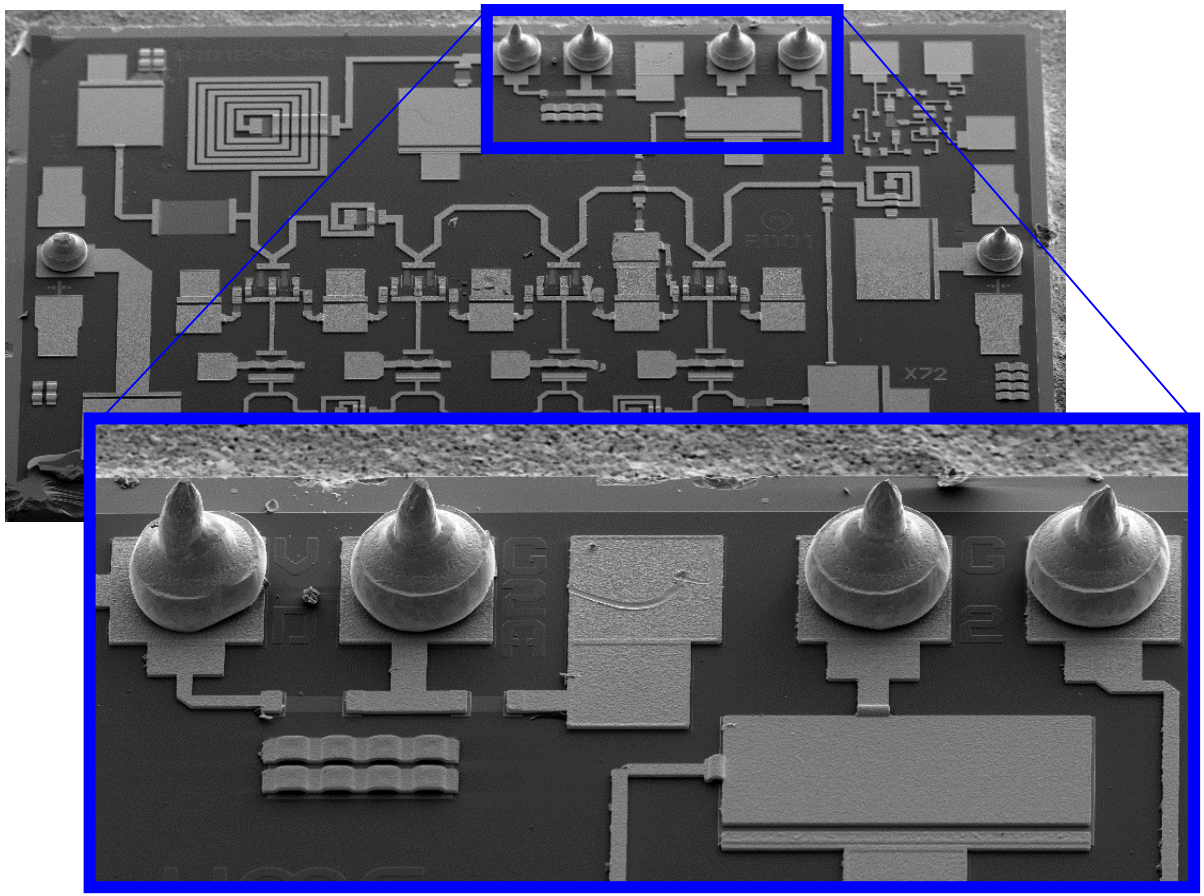
- **To Embed active die on Flex**



- **To provide working demonstrators**

- **To evaluate reliability**

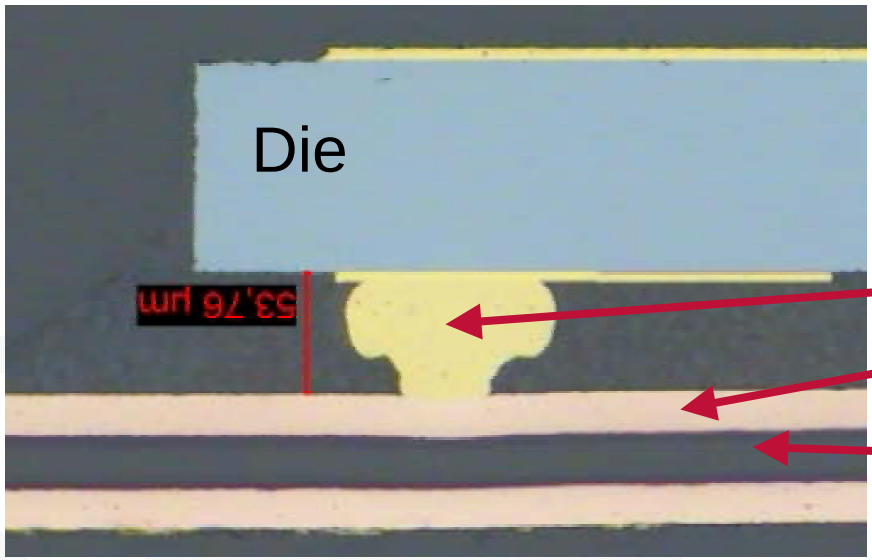
Stud Bump the die

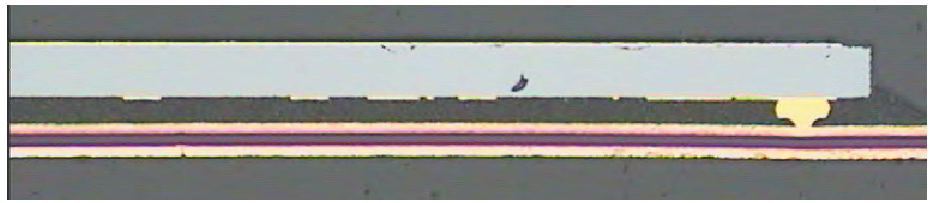


(Use solder bumps at higher volumes?)

Image:- courtesy of Thales

Assemble die to Flex





Gold stud bump

Copper tracking

Flex

- **Thermo compression bond die to flex substrate**
- **(Reflow solder solder bumps at higher volume?)**

Laminate flex/die with Prepregs

Prepreg

Prepreg with machined holes

Polyimide Flex substrate

Create Vias

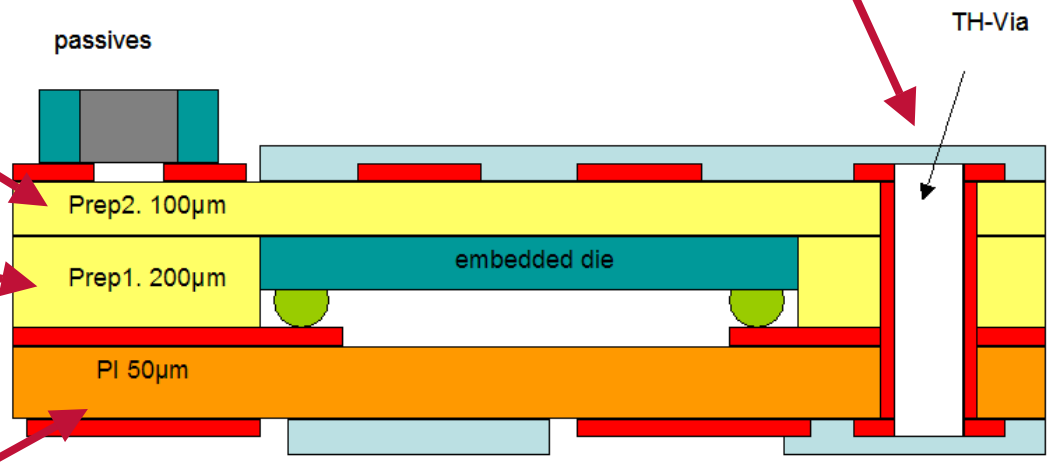
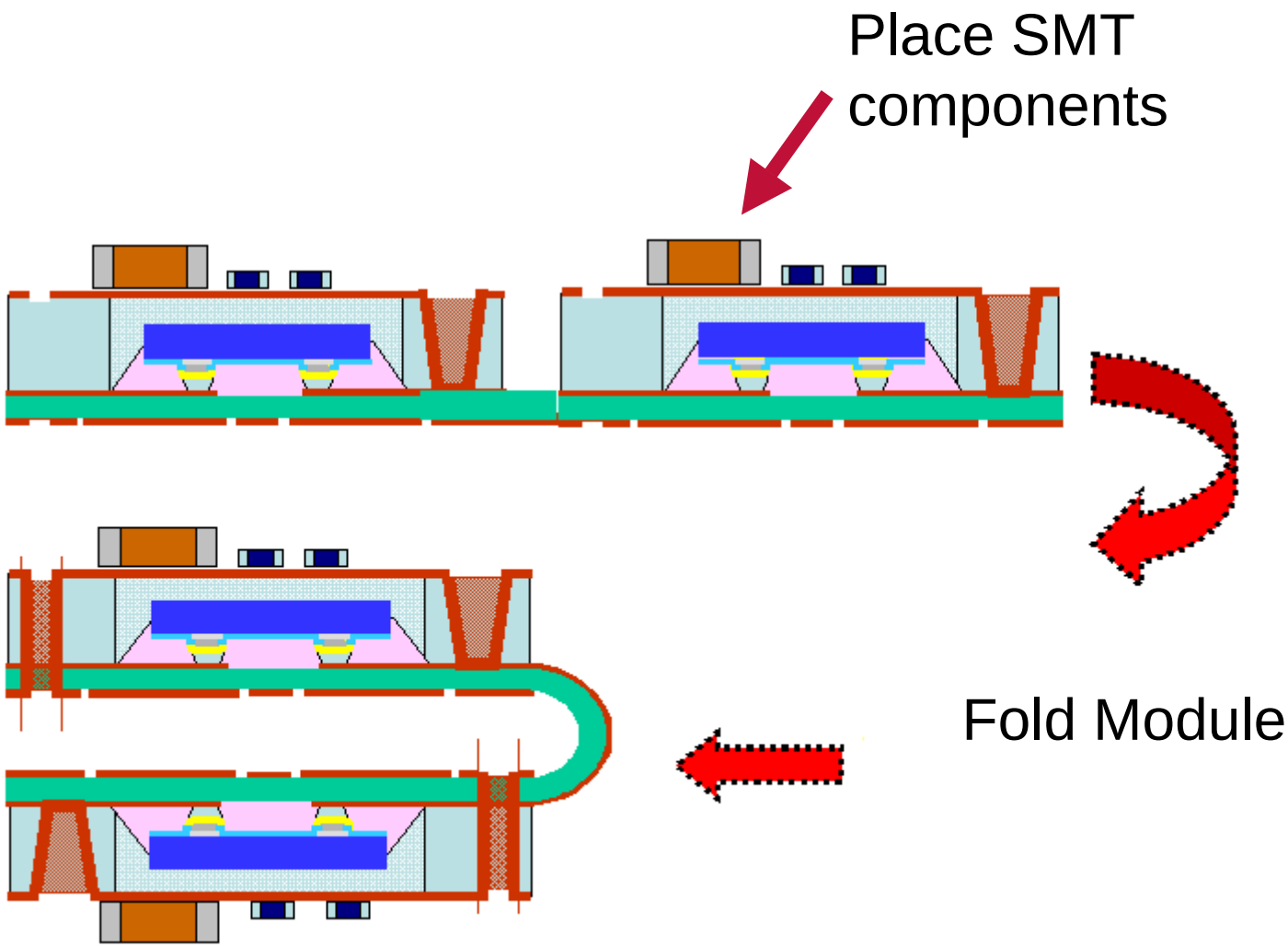


Image:- courtesy of RL Design

Final Assembly



Will SHIFT meet Zarlink RF module objectives?

- **Space / Format**
  - it will reduce module size
  - Will suit module with flex tail

- **Reliability**
  - Testing not yet started
- **RF shielding / component protection**
  - Partial shielding and component protection - might require a shield
- **Reduced cost**
  - Known Good Die issue / Novel process – low yields?
  - Limited supplier base – higher cost

CiP
Chip in Polymer

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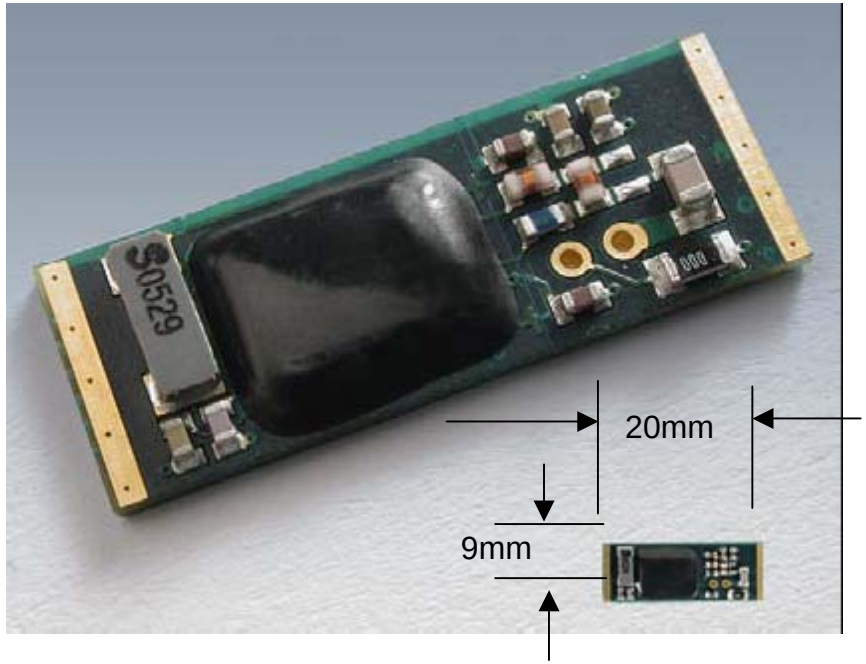
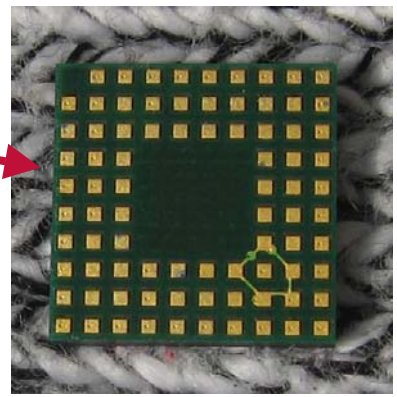
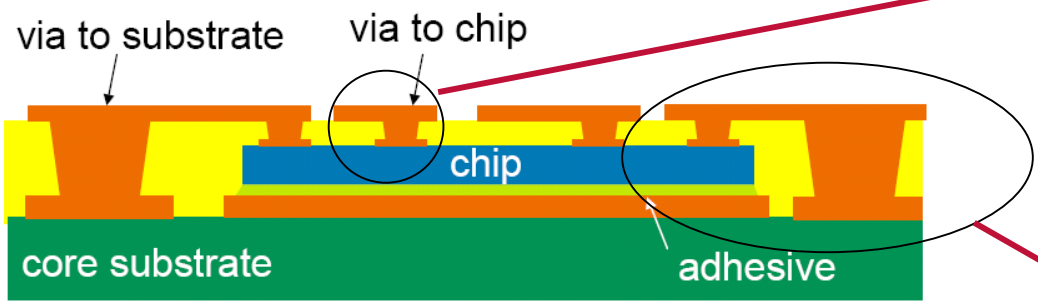
Objectives of CiP

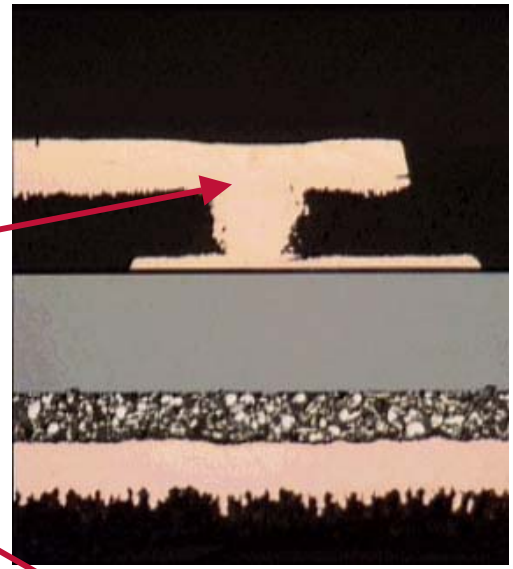


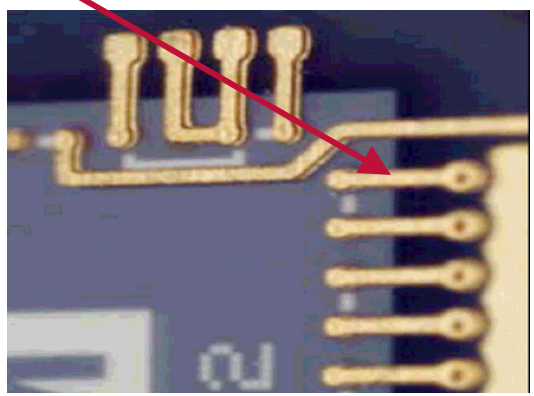
- **Reduce RF module SiP to less than half the current size**
- **Surface mountable LGA format**
- **Demonstrate a working RF transciever**



CiPs structure





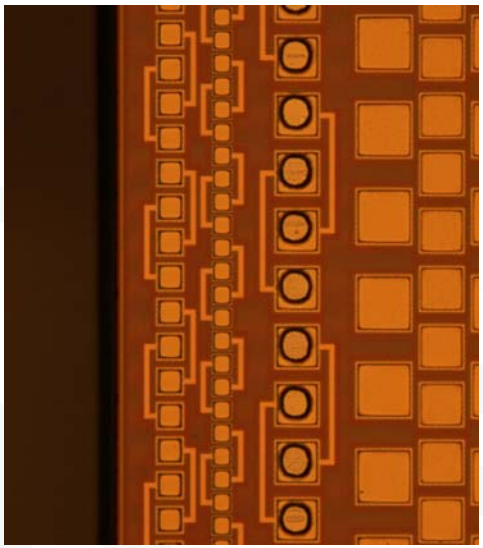


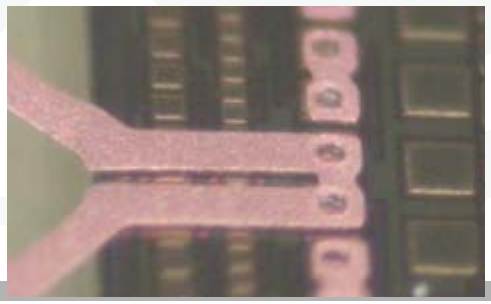
- **Based upon FR4 core**
- **Plated via connections to die**

Pictures courtesy of TUB

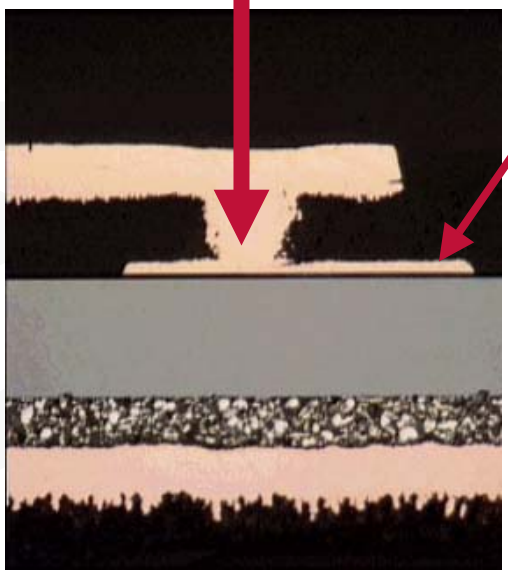
Plate the die wire bond pads

- **Bond pads must be plated to “stop” the laser beam**





Laser beam drills
to create via hole



Electroless Ni/Au

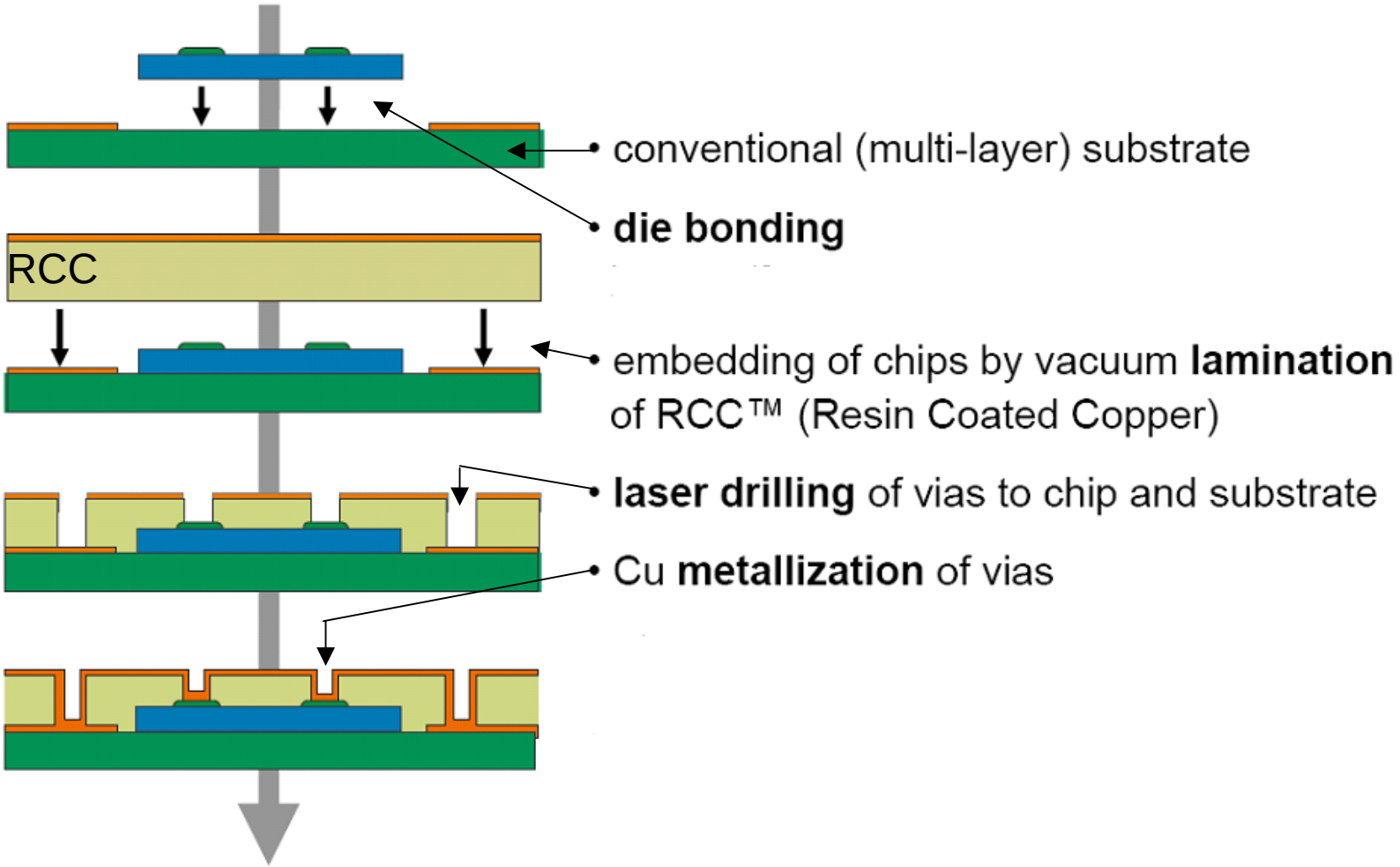
Or

Electroplated Cu

Pictures courtesy of TUB and IMEC

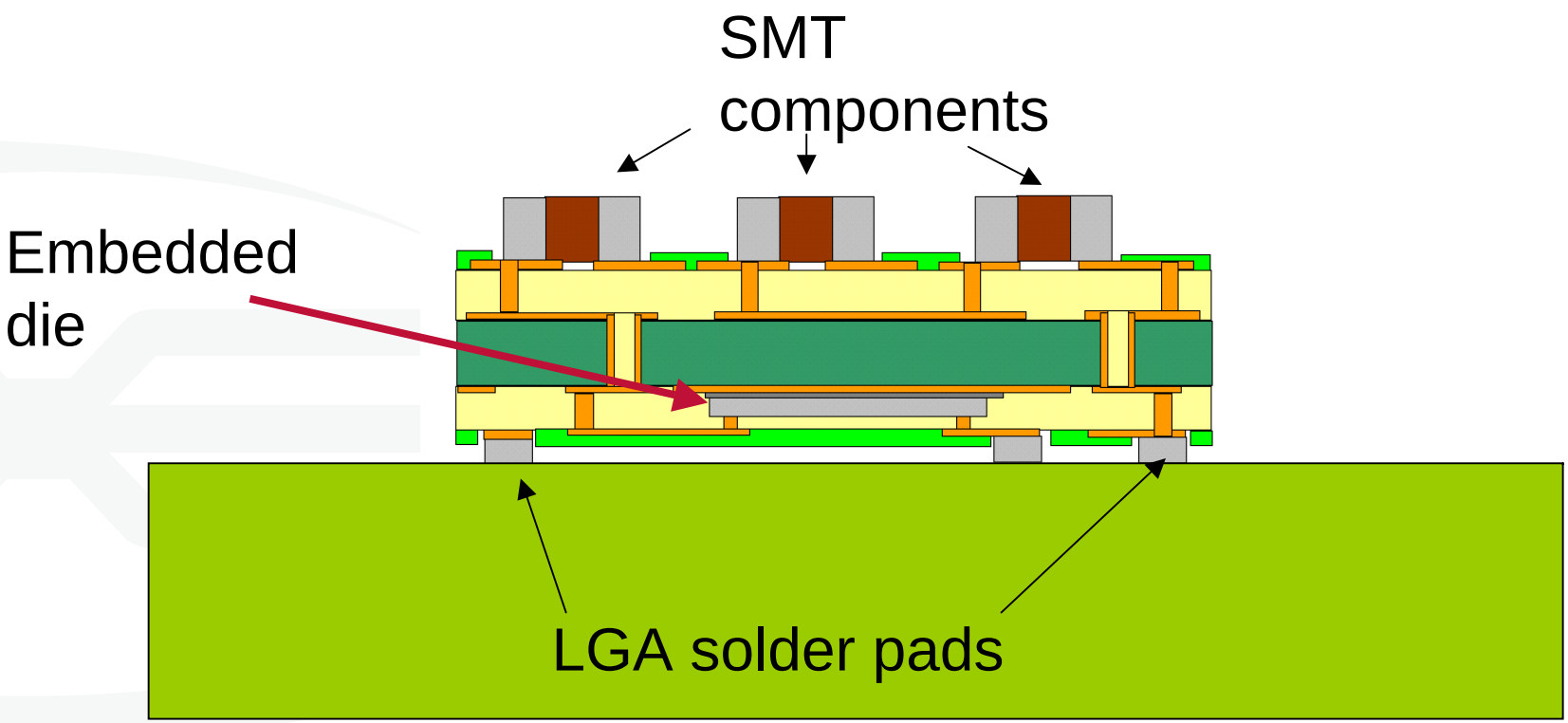
CIPS embedded die

Chip in Polymer – Basic Process Flow

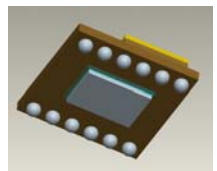


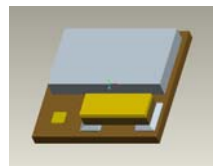
CiPS module

- **SMT module**
- **Working RF module**



Will CiP meet Zarlink RF module objectives?





- **Space / Format**
  - it will reduce module size
  - Will suit low profile SMT format
- **Reliability**
  - 3000 thermal cycles
  - Vibration and shock
  - MSL 3, MSL 2 soon
- **Reduced cost**
  - Extra cost to plate the die pads
  - Known Good Die issue / Novel process – low yields?
  - Limited supplier base – high prices?

Alternative embedded passive component technologies

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Embedded resistors and capacitors

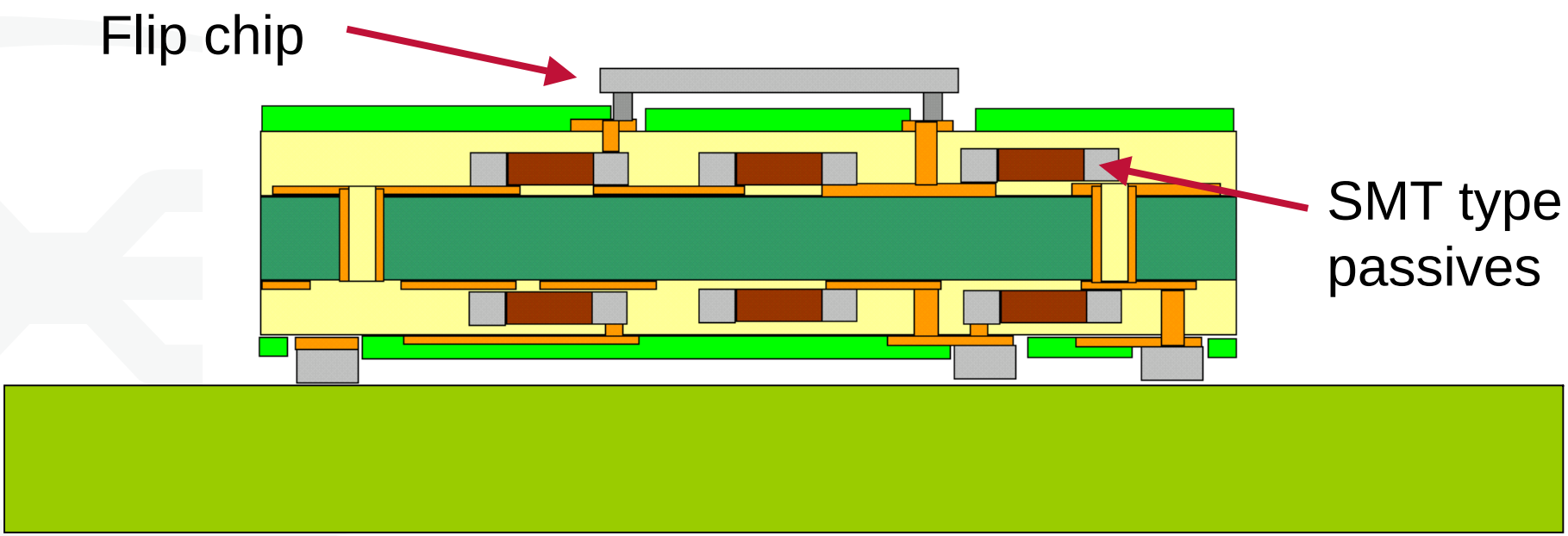
- **Laminate layer capacitors and resistors are available**
- **Compatible with PCB manufacturing techniques**

- **Resistors**
  - Good for PCBs with many resistors with wide tolerances
  - Zarlink circuits have no or few resistors

- **Capacitors**
  - Good for decoupling ground/ power planes on large PCBs
  - Capacitance too low for Zarlink

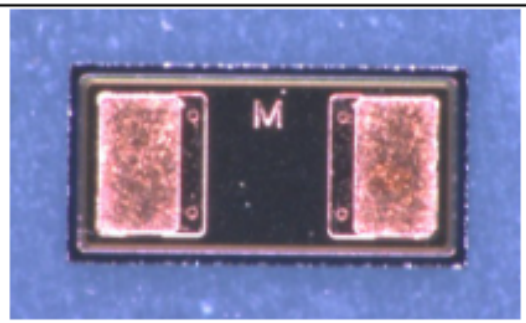
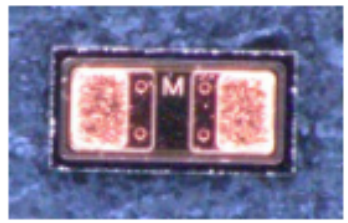
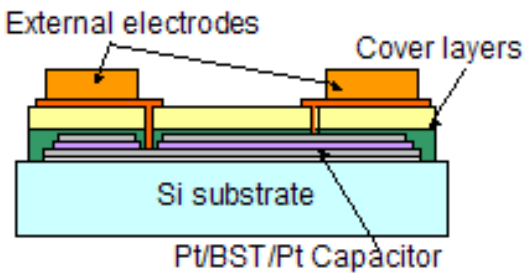
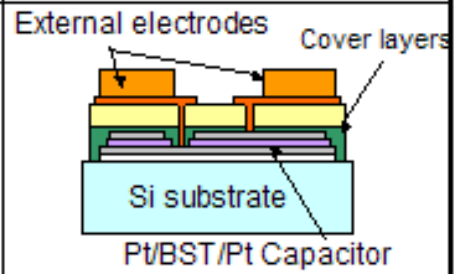
Embed SMT type passives?

- **This structure is currently used in products in Japan**
- **PCB yield loss involves cheap passives and not die**
- **Would costs be lower?**



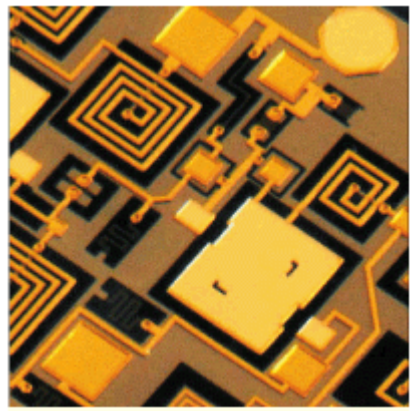
Murata Embeddable Passives

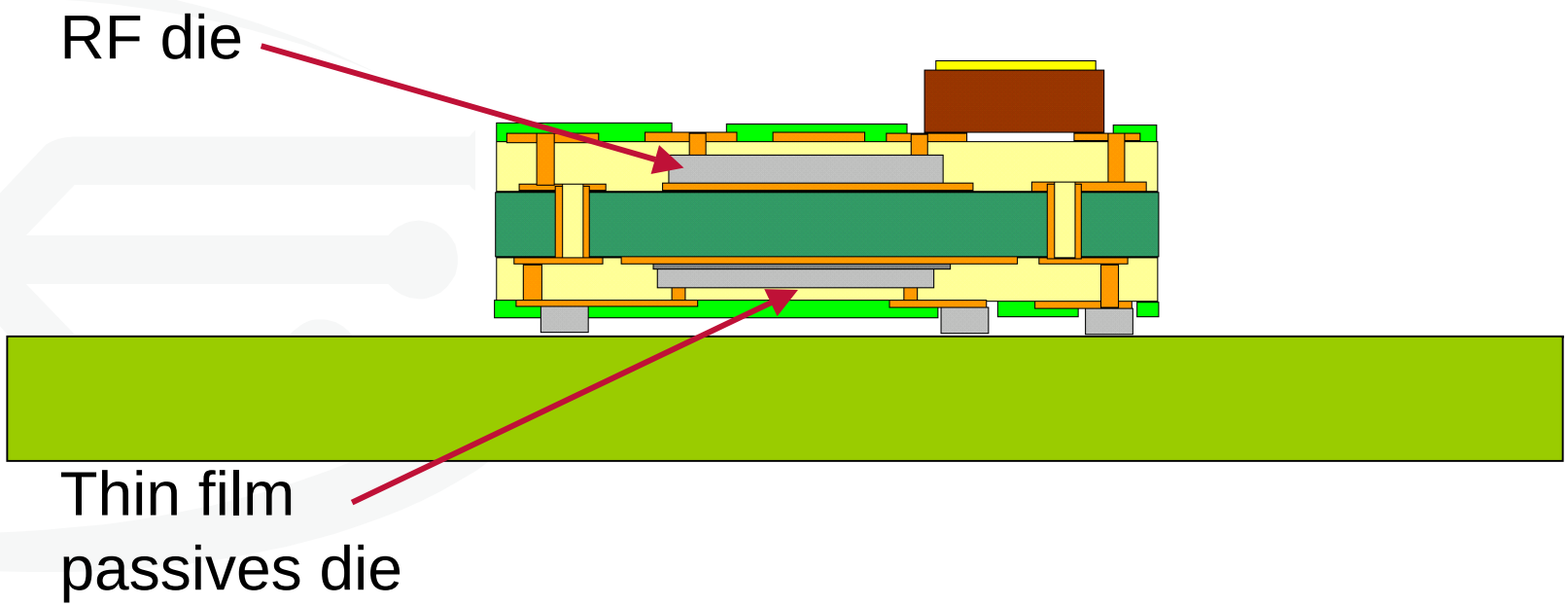
muRata **Under Development**

Size	1.0 mm x 0.5 mm (0402)	0.6 mm x 0.3 mm (0201)
Thickness	~ 100 - 50 µm	~100 - 50 µm
Appearance		
Cross-sectional outline		
Capacitance at 1kHz	15.5 nF	4.2 nF
Dissipation factor at 1kHz	2.4 %	2.4 %
Insulation resistance at 4V	160M-ohm	640M-ohm

Integrate thin film passive IC

- **Die with thin film passives on it surface**
- **Embed two die to produce smallest format?**
- **Lowest yield format – expensive?**





Conclusion

- **PCB, IC and SMT technology are converging**
  - Zarlink intends to understand these new design technologies
- **Currently the supply chain is immature**
  - Few suppliers
  - Equipment needs developing (eg large area pick and place machines)
  - Specialist passives need developing for embedding
- **Zarlink is investigating embedded components for SiP**
  - to enable miniaturisation
  - but high yields and lower costs need to be demonstrated

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