

**WHITE PAPER**

# **The Future of Timing: The Transition to Packet Networks**

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As published in Electronic Engineering and Product World  
January 2007



As the telecommunications network transitions from circuit to packet technologies, network timing and synchronization will need to evolve to support the new IP-based infrastructure.

Today there are clearly defined standards governing circuit-switched network synchronization, from SONET/SDH down to PDH T1/E1 rates, and well understood building blocks to deploy or enable network synchronization at the system, board and component levels.

However, as networks evolve to a packet-based infrastructure, timing and synchronization requirements will change significantly. Work is already underway within the standards bodies and working groups to develop equivalent mechanisms to support packet-switched synchronization technologies. These may be at the Layer 1 level with physical layer synchronization, at the Layer 2 level with Ethernet switched technologies, or the Layer 3 level with IP routed technologies.

While the “all-IP” world will eventually be a reality, for an extended period of time synchronization will need to support a hybrid of both the older circuit-switched and the newer packet-based timing interconnections. This article discusses the transition of timing and line card synchronization to support hybrid circuit and packet networks. It will focus on the board and chassis level, and demonstrate how synchronization may be received from the network and how clocks can be routed internally to the system.

## TDM Timing Card

The main component on a timing card in most circuit-switched TDM equipment is a digital phase-lock loop (PLL) capable of meeting the relevant timing and synchronization standards from the ITU-T, ANSI and Telcordia.

The TDM timing card is responsible for delivering standard compliant system clocks to the line cards. Most systems will contain two timing cards in order to provide redundancy and ensure reliable, uninterrupted synchronization throughout the system. The most common applicable timing standards for T1/E1 equipment are Telcordia GR-1244-CORE for North American T1/DS1 equipment, and ITU-T G.813 option 1 for E1 equipment outside North America.

Using the Telcordia GR-1244-CORE specification as an example, clock quality is characterized by Stratum levels, ranging from Stratum 1 as a PRS (primary reference clock) down to Stratum 4 at the CPE (customer premise equipment). Typically, system clocks in CO (central office) equipment would be of Stratum 3 or 3E quality.

The main requirements for a TDM PLL on a timing card are holdover, controlled reference switching, phase transient tolerance, wander/jitter transfer, wander/jitter tolerance, and wander generation. Jitter generation, because it is very application-dependant and it is difficult to distribute very low jitter clocks across the backplane to the entire system, is typically handled on the line card PLL.

With the traditional circuit-switched timing card, the TDM PLL selects from among a variety of clock input options. First, the TDM PLL may select a BITS/SSU synchronization source recovered through the on-board LIU (line interface unit), which provides either a 1.544 MHz or 2.048 MHz reference clock for use in external timing mode. Second, the TDM PLL may select one of the 8 kHz references from the backplane, which are provided as recovered clocks by the line cards in the system for use in line timing mode.

In a redundant system the timing card may also be required to select the backplane systems clocks from the other timing card. In this type of redundant architecture, one of the timing cards is designated as the mas-

ter and the other as the slave. The master (or active) timing card selects one of the network references (line timed or externally timed). The slave (redundant) timing card selects the master system clocks and closely tracks these clocks to provide redundant system clocks that are both frequency and phase aligned to the master. In the case of a failure on the master timing card, the slave timing card assumes the role of master. This is common in systems where the backplane specification requires tight phase alignment between the system clocks, such as ATCA and H.110.

Once the TDM PLL has selected its reference it will drive the backplane with a clock and frame pulse to be used by all the line cards in the system.

## Hybrid TDM and Packet Timing Card

Figure 1 outlines a timing card that is capable of performing clock and synchronization requirements for both circuit- and packet-switched networks.

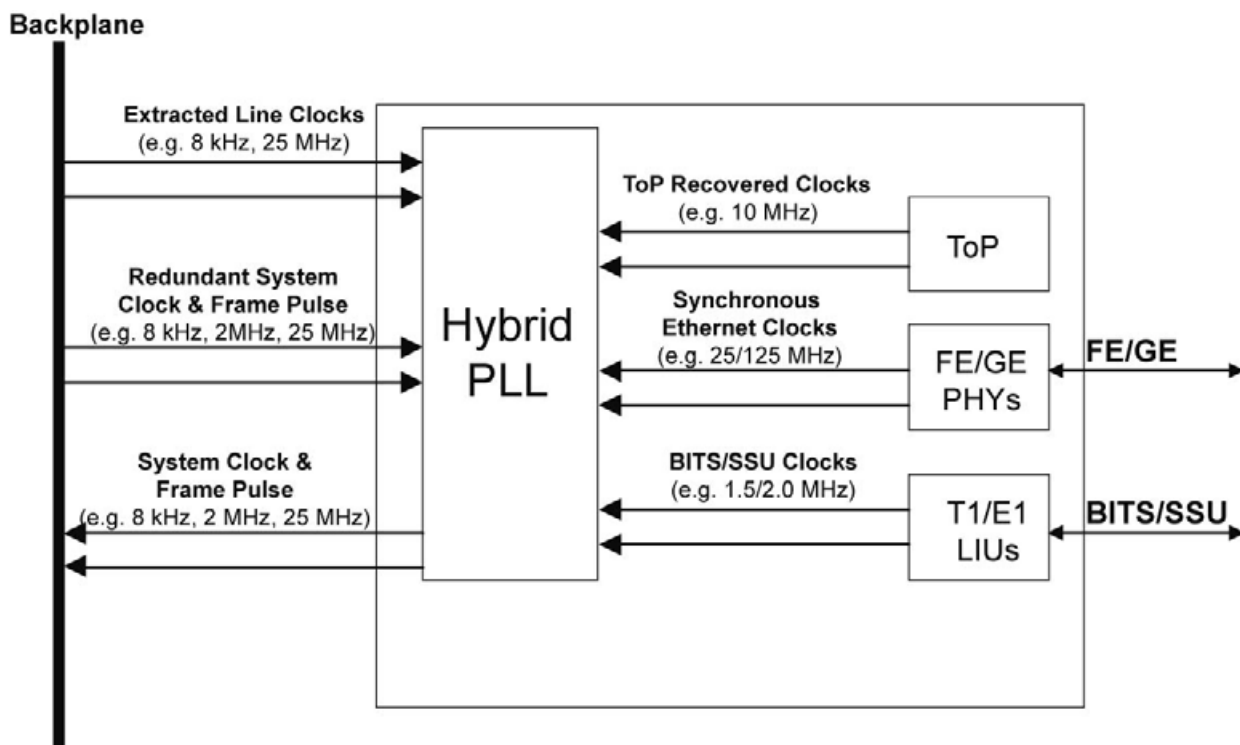


Figure 1: Dual TDM and packet timing card

The timing card will now be populated with a hybrid PLL that supports more synchronization options than its TDM PLL predecessor. The hybrid PLL now supports new input frequencies as well as up to five choices for clock references:

- The legacy SSU/BITS input remains to provide either 1.544 MHz or 2.048 MHz clock reference;
- The clock extracted by the various line cards in the system. If the line cards interface to TDM networks then they will likely provide an 8 kHz reference. If the line cards interface to packet networks (for example, with Ethernet interfaces), they may still provide an 8 kHz reference frequency, dividing 25 MHz by 3125;

- System clocks from the redundant timing card that are used as a reference to provide phase-aligned, frequency-locked redundant system clocks to the system;
- If there is a synchronous Ethernet interface on the timing card, the Fast Ethernet (FE) or Gigabit Ethernet (GE) PHY may provide an extracted 25 MHz or 125 MHz clock reference to the hybrid PLL;
- Again, if there is an Ethernet or IP interface on the timing card, the timing card may support timing-over-packet (ToP) technology, such as RTP, IEEE 1588 or NTP. The timing-over-packet device shown would receive Ethernet or IP packets, and perform adaptive clock recovery to provide the hybrid PLL with a reference source.

Once the hybrid PLL has selected a reference source, it must be capable of providing not only the TDM clock frequencies of 8 kHz, 1.544 MHz and 2.048 MHz, but also Ethernet clock frequencies such as 25 MHz and 125 MHz.

Optionally, the hybrid PLL may internally include the timing-over-packet engine. If this is the case, then the hybrid PLL supports clock and composite clock interfaces, as well as a packet interface.

## TDM Line Card

Figure 2 shows a simplified line card used in TDM equipment today supporting circuit-switched networks. For simplicity, let's assume this line card is used to provide NxDS0 voice service over a T1/E1 line. The PLL on the line card may include either a digital PLL, and analog PLL, or both.

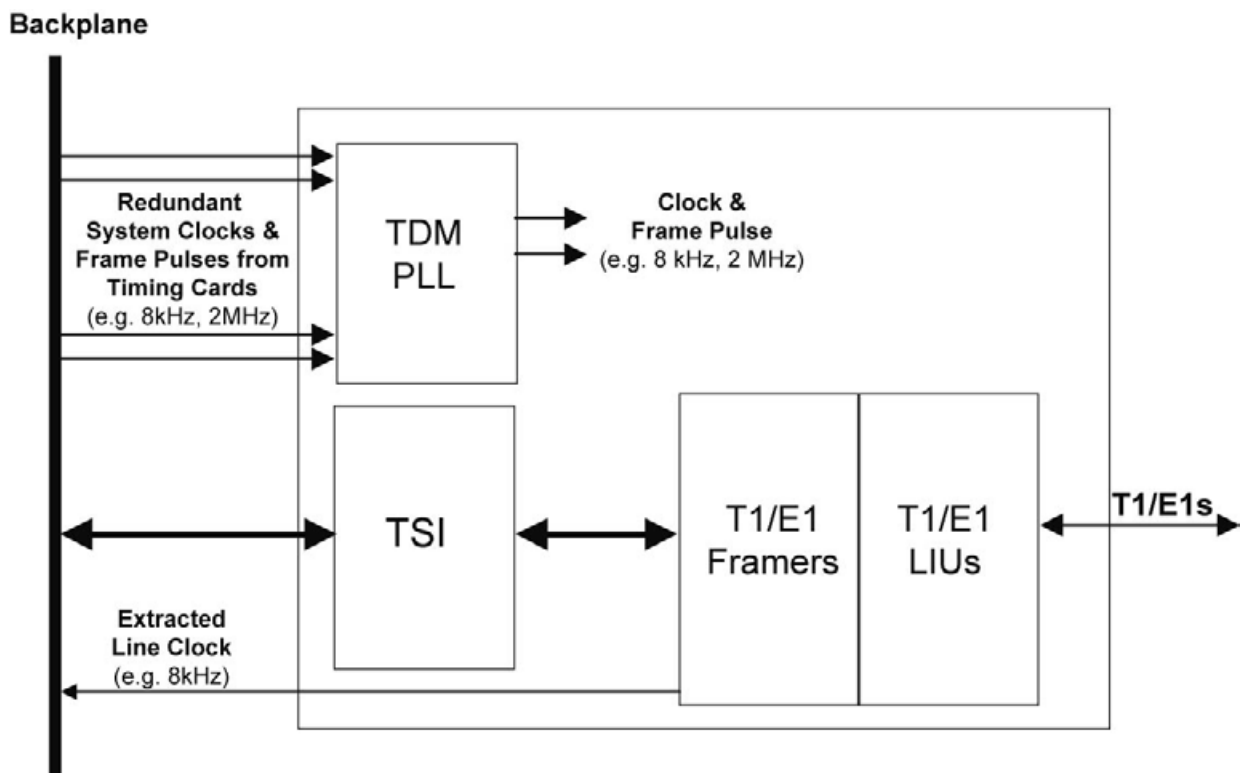


Figure 2: TDM line card

The main requirements for a PLL (whether DPLL, APLL or both) on a line card are to monitor the incoming system clock from the timing cards and perform hitless reference switching in the case of failure. The line card PLL must also perform jitter attenuation in order to supply low jitter clocks to the line card devices to ensure error-free and standard compliant operation.

The line card PLL locks to the backplane reference clock from one of the timing cards, shown previously. It will then generate all necessary frequencies on the line card for the TSI, framer and LIU. These frequencies are usually 8 kHz, 1.544 MHz and 2.048 MHz. It is assumed the backplane reference clocks are 8 kHz and 2 MHz.

The line card may also extract a timing reference from the T1/E1 line and provide this to the timing card. Normally this would be an 8 kHz frequency reference.

### Packet Line Card (Retrofit)

Figure 3 is a simplified line card that has Ethernet interfaces, but continues to fit into the existing system backplane setup for a traditional TDM line card. The clock and data interfaces remain unchanged on the backplane. The NxDS0 data continues to be carried through a TSI and the extracted line card clocks and the backplane timing card clocks remain 8 kHz and 2 MHz.

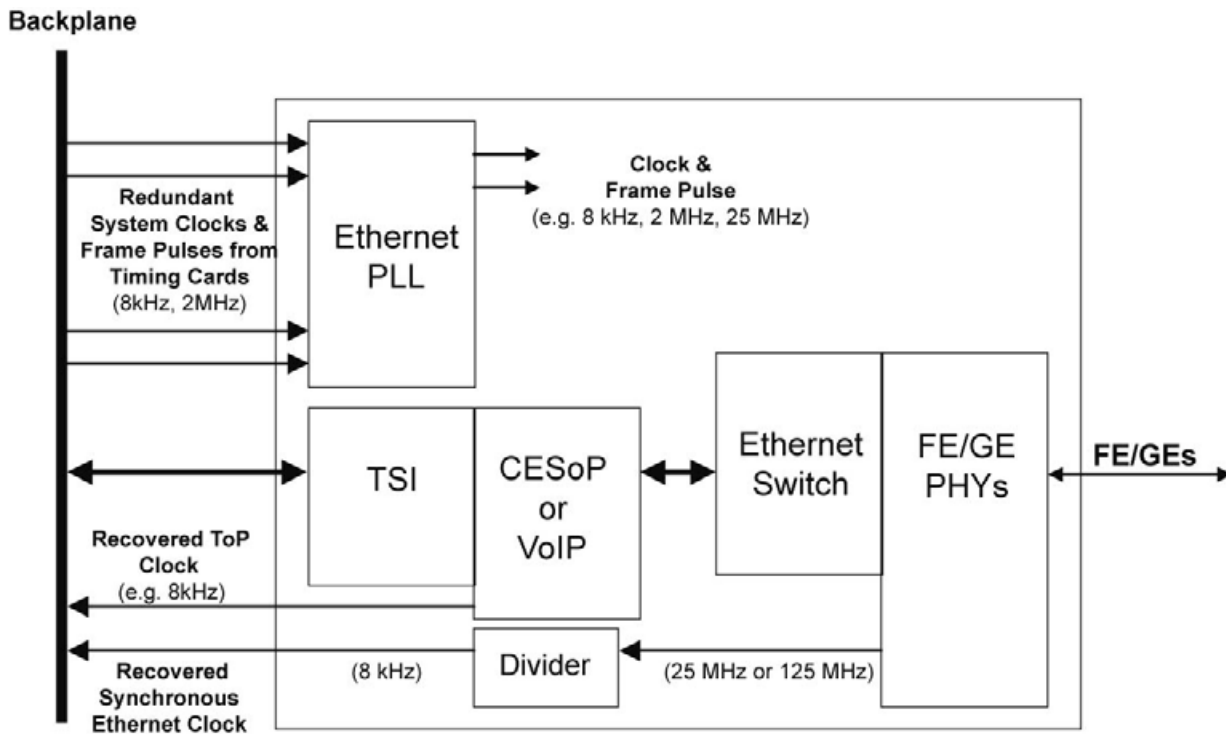


Figure 3: Packet line card (retrofit)

On the line card itself, however, the VoIP or CESoP (circuit emulation services-over-packet) processor in conjunction with an Ethernet switch and FE/GE PHY carries the NxDS0 voice service over an Ethernet/IP network.

With respect to timing, the retrofit PLL must lock to a traditional TDM frequency from the timing card, and generate both TDM clock frequencies and packet clock frequencies such as 25 MHz. In terms of performance, the packet clock frequencies used for physical layer synchronization will require significantly better jitter performance than pure TDM frequencies. This adds additional burden on the retrofit PLL in terms of jitter generation and attenuation.

From the backplane to network interface, there are many possible timing paths. First, the retrofit PLL could generate 25 MHz for the FE/GE PHYs to provide physical layer synchronization. Second, the retrofit PLL could generate 8 kHz or 1.544 MHz/2.048 MHz for the CESoP or VoIP processor, which in turn could generate packets with embedded timing information to the packet network.

From the network to the backplane, there are again a variety of possibilities for timing paths. First, the FE/GE PHYs could extract a 25 MHz or 125 MHz clock from the physical line, which is then divided down to 8 kHz and provided to the timing cards over the backplane. Second, the CESoP or VoIP processor could perform adaptive clock recovery on incoming packets with embedded timestamps and provide the reference clock for the backplane.

### Packet Line Card (New)

Figure 4 depicts equipment that is purely packet-based, without the legacy TDM backplane. In this scenario the clocking is more likely to be based solely on 25 MHz (or multiples thereof). The block diagram outlines a packet line card with GE/FE interfaces.

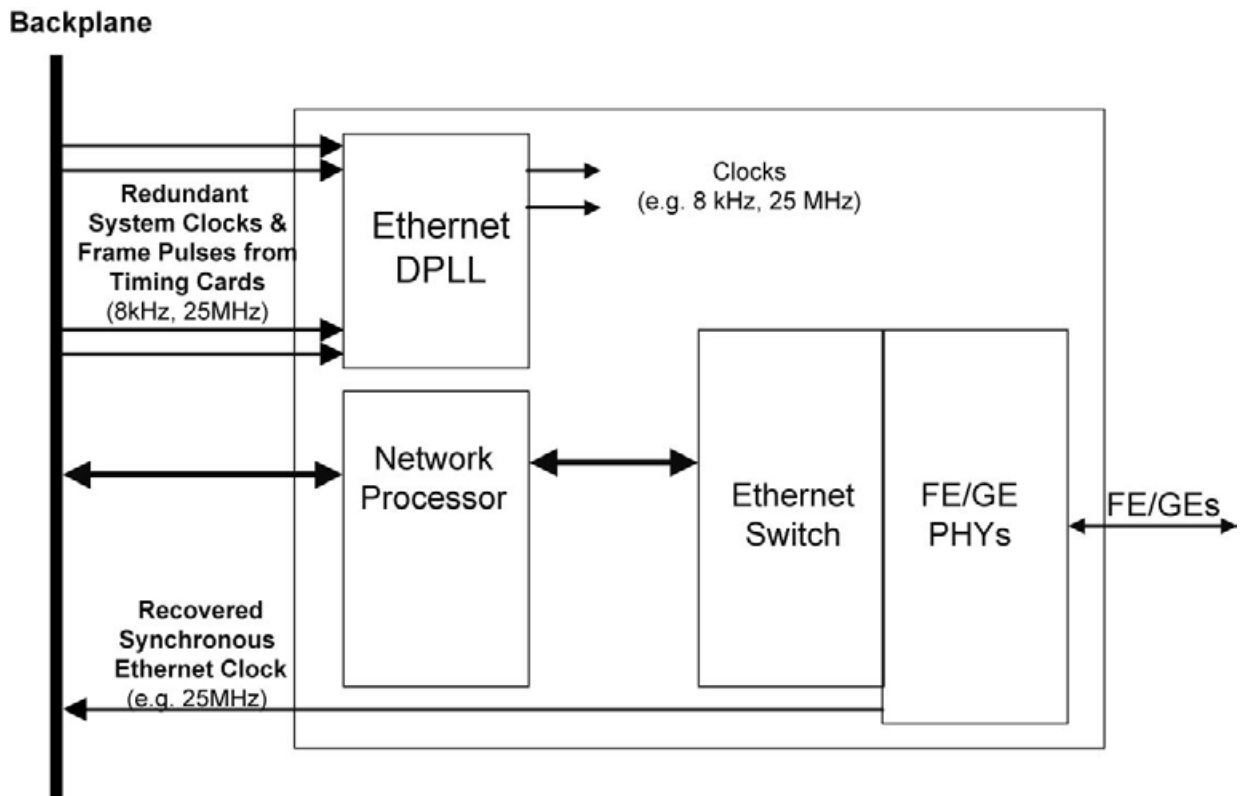


Figure 4: Packet line card (new)

The FE/GE PHY extracts a 25 MHz or a 125 MHz frequency from the physical layer and provides that as a network reference to the timing card. The timing card in turn selects one of the line card references, cleans the clock, and provides a common 25 MHz (and possibly 8 kHz) clock to all line cards.

The Ethernet PLL will lock to the 25 MHz clock and provide all necessary clocks for the line card. In addition, it may provide a 25 MHz clock used by the PHY to time the Ethernet physical layer to provide timing synchronization to the next node in the network.

## Summary

Previously, the evolution of synchronization was incremental and driven primarily by increasing bandwidth and clock rate. However, as networks evolve from a circuit- to packet-based infrastructure, the timing and synchronization of telecommunications networks will undergo a significant change.

The clock engines and clock interfaces in packet-based equipment will need to support a variety of new timing options. There will be a combination of Layer 1 techniques using the physical layer, as well as Layer 2 switched and Layer 3 routed techniques. These new synchronization methods are already underway with improvements to IEEE 1588 and NTP specifications to support telecommunication network requirements.



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