



Carrier Grade Synchronization Architecture in ATCA

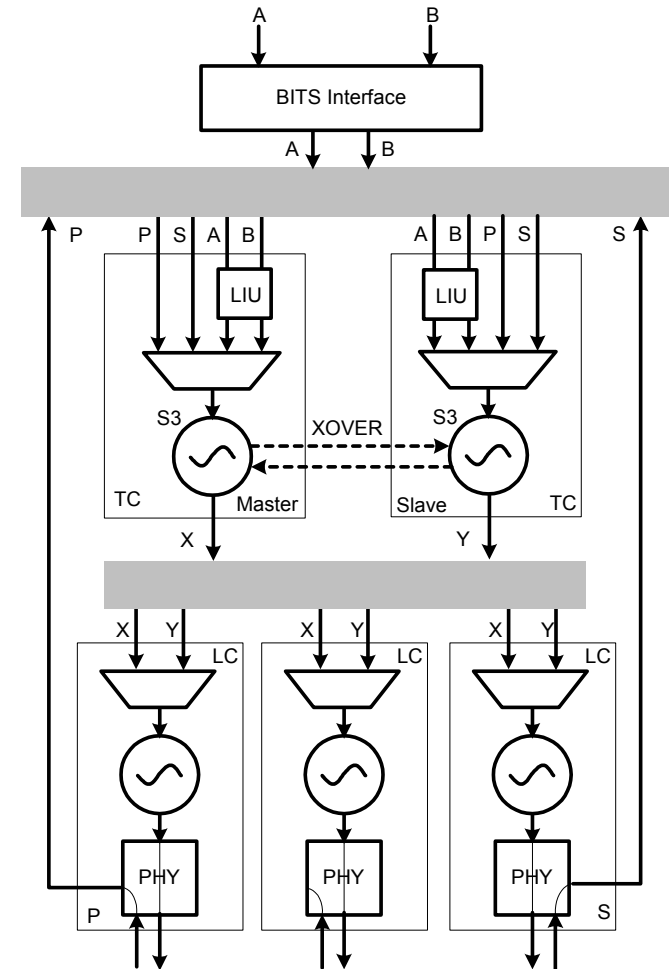
Daniel Gallant
Timing System Architect

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Key Features Of A Carrier Grade Synchronization Architecture

- ✓ Redundant timing sources
- ✓ Isolated master/slave crossover bus
- ✓ References are terminated even when both timing cards are removed
- ✓ Each timing card has access to all references even when the other timing card is removed
- ✓ Removal of a removable unit will not cause a non-compliant phase transient or cause a reference switchover
- ✓ S/W control of time insensitive functions (i.e. configuration, status)
- ✓ H/W control of time sensitive functions (i.e. automatic failure mechanisms)



ATCA Synchronization Signals

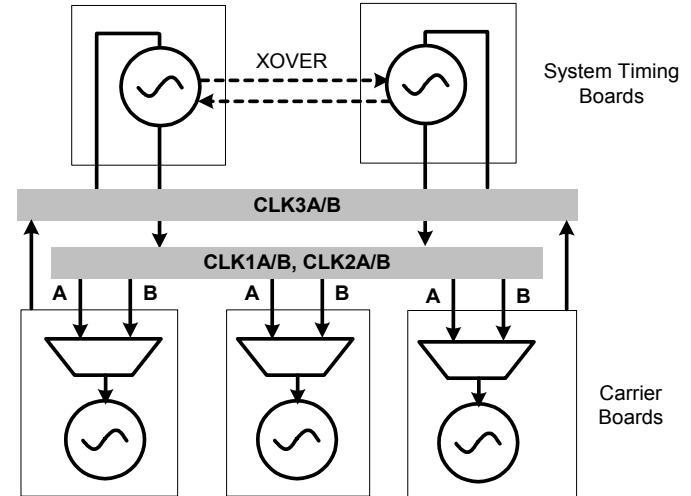
- Six Clock Buses divided into 3 groups
 - **CLK1A/B** - 8kHz clock or frame pulse with 122ns min pulse width
 - **CLK2A/B** - 19.44MHz clock
 - **CLK3A/B** user defined clock (<100MHz) or network reference (8kHz, 1.544MHz, 2.048MHz, or 19.44MHz)
- CLK1A/B must meet **Stratum 4E** requirements
- CLK2A/B must meet **Stratum 3 or 3E** requirements
- Phase difference between A and B busses of CLK1 and CLK2 < **10 ns** (requires master/slave timing sources)
- Clocks are distributed using **MLVDS** drivers/receiver using a multi-drop configuration

ATCA Synchronization Architectures

■ Centralized Timing Architecture

- A pair of redundant system timing boards provides timing to all the carrier boards
- System timing boards ensures standards compliance (e.g. GR-1244 Stratum 3, GR-253 Stratum 3/3E, G.813 Opt 1, 2, etc...)
- Carrier boards select one of the system timing references to generate its own clocks for AMCs, etc...
- Provides redundant timing paths necessary for carrier grade networks

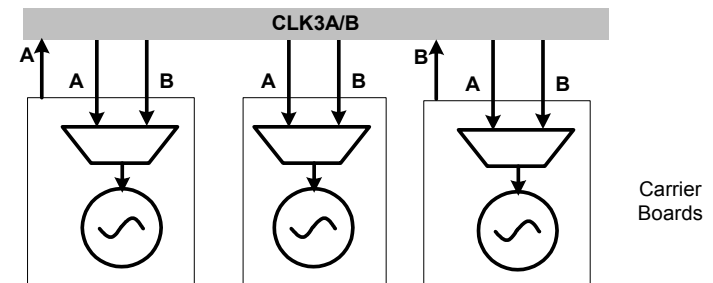
Centralized Timing Architecture



■ Distributed Timing Architecture

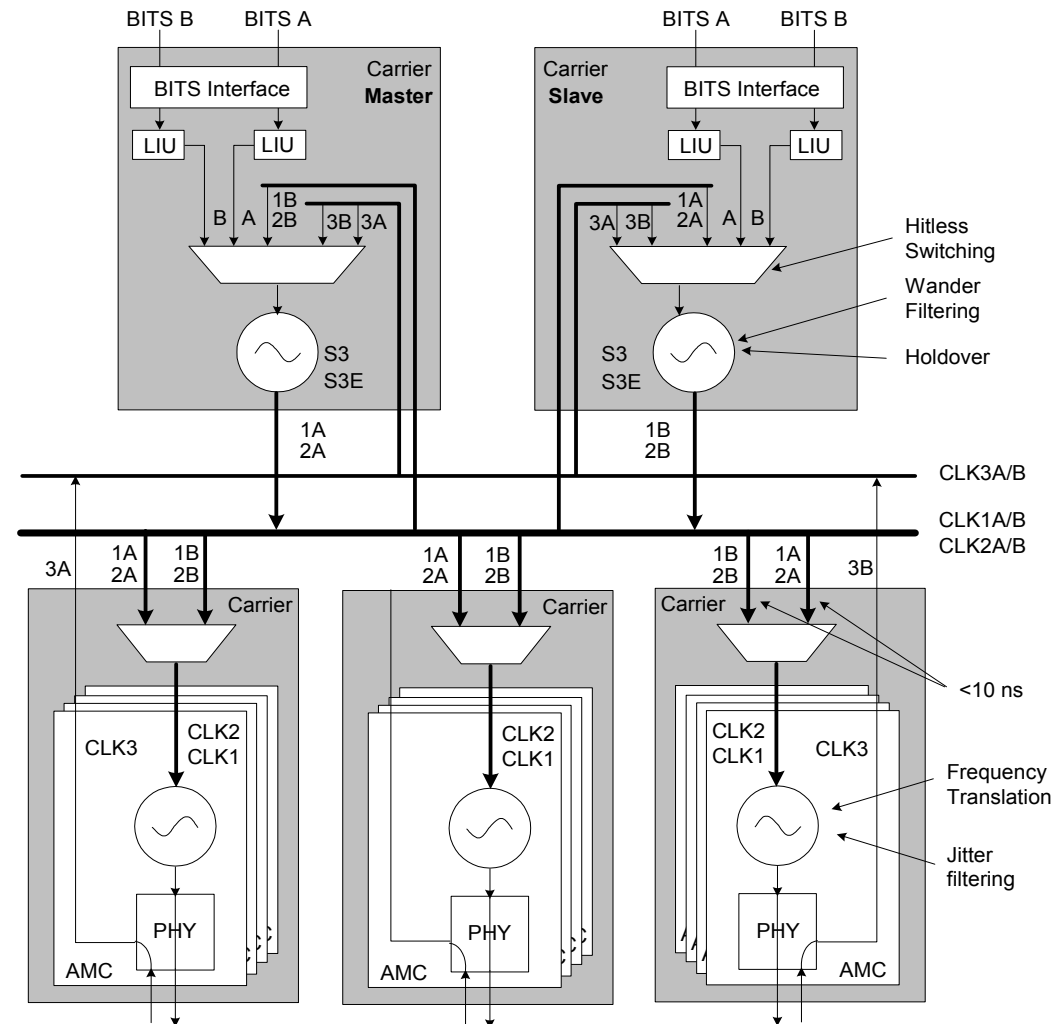
- The system timing function is distributed across all the carrier boards
- Carrier grade reliability is still possible with proper clock management and design

Distributed Timing Architecture

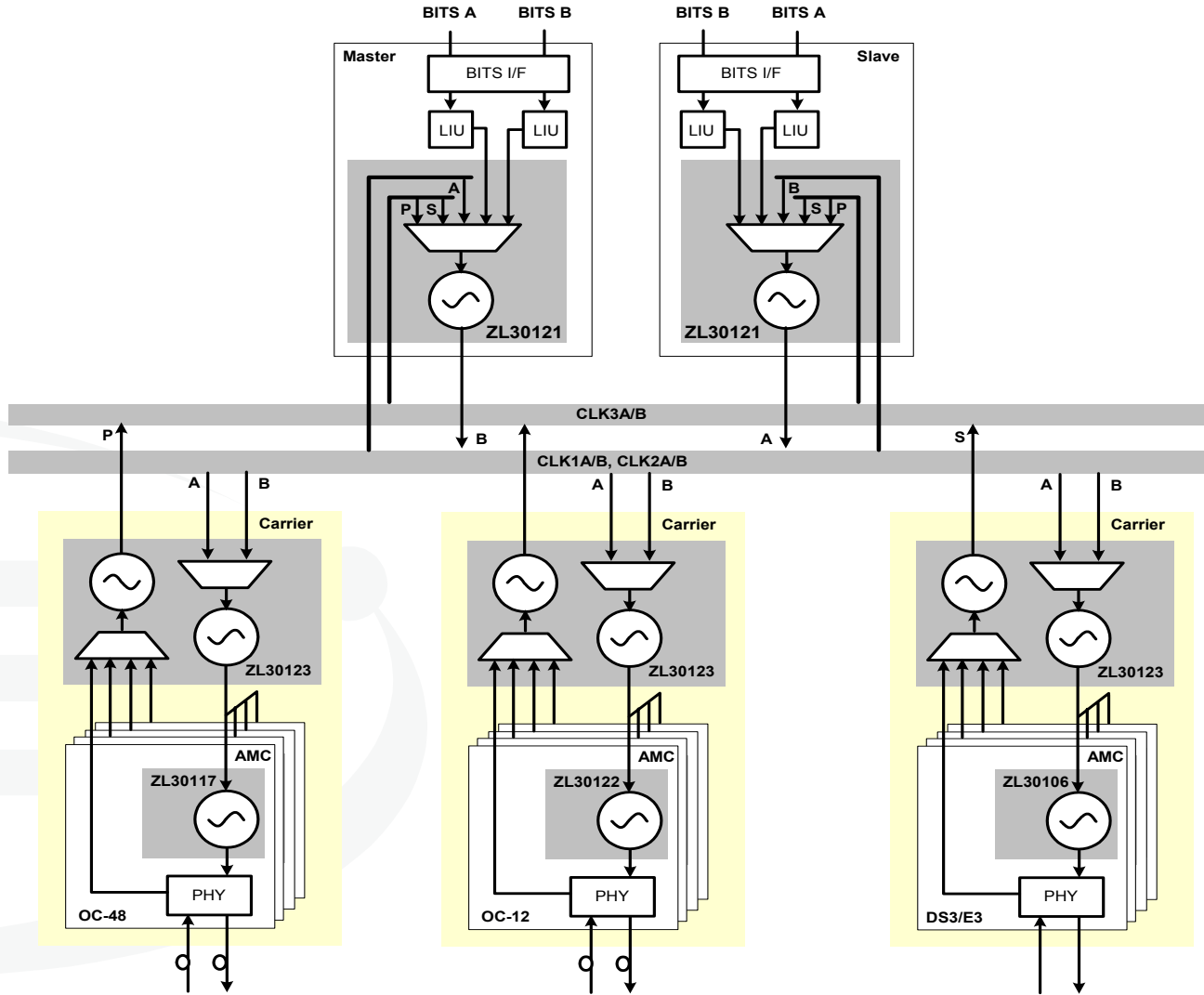


ATAC Centralized Sync Architecture

- ✓ Redundant timing sources
- ✗ Isolated master/slave crossover bus (not critical)
- ✗ References are terminated even when both timing cards are removed (option to locate on the RTM)
- ✓ Each timing card has access to all references even when the other timing card is removed
- ✓ Removal of a removable unit will not cause a non-compliant phase transient or cause a reference switchover

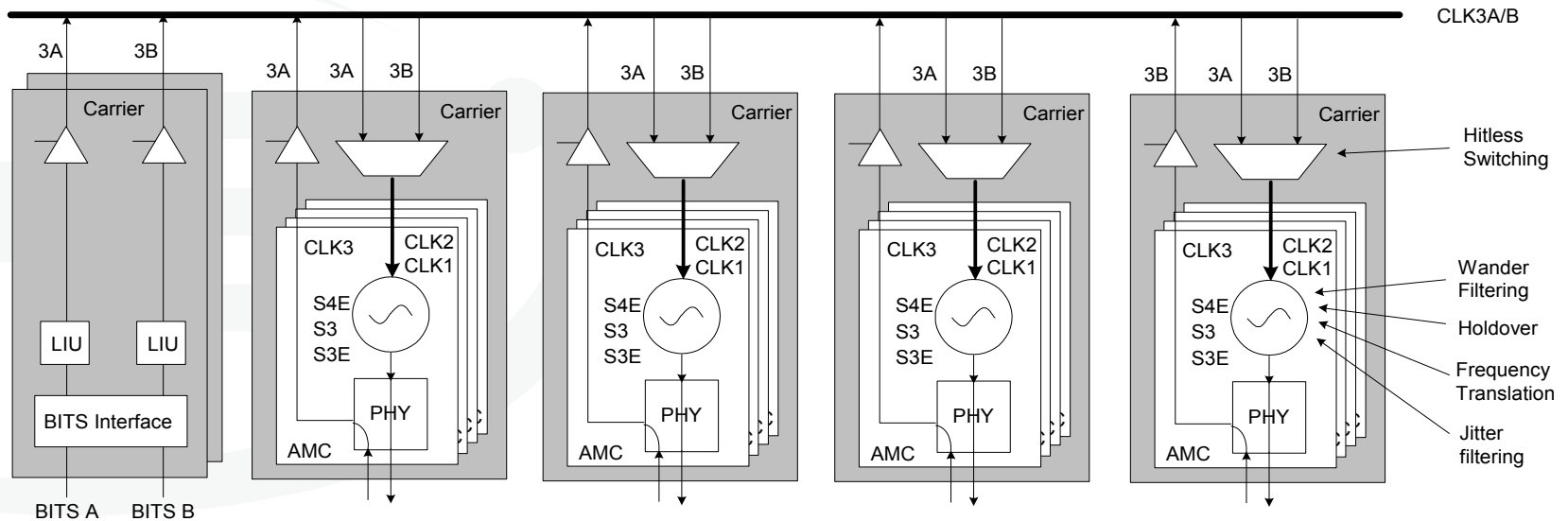


ATCA Centralized Timing Implementation

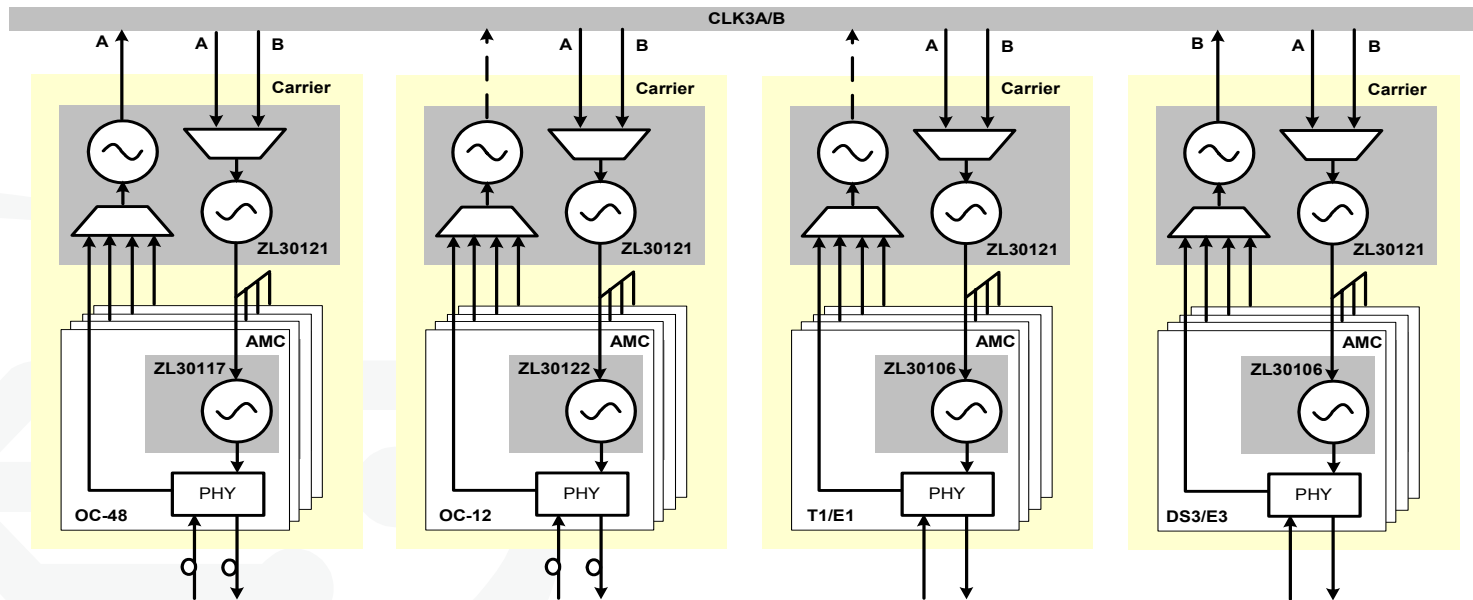


ATCA Distributed Sync Architecture

- Timing source redundancy is not required since every card is its own timing source
- Unknown phase relationship between CLK3A and CLK3B bus makes hitless switching a must!
- Economical for multi-functional systems that have limited slots requiring synchronization
- Makes upgrading system wide clock performance more difficult (e.g. S3 to S3E)



ATCA Distributed Timing Implementation



Summary of Timing Devices for ATCA

■ System Timing Boards

- ZL30105 - GR-1244 Stratum 3 Compliance
- ZL30121 - GR-253 Stratum 3 Compliance
- ZL30130 - GR-1244 Stratum 3E Compliance (pin compatible with ZL30121)

■ Carrier Boards

- ZL30123 - Bi-directional timing path PLL, clock selector, hitless switching

■ AMC

- ZL30106 - T1/E1, DS3/E3, OC-3/STM-1
- ZL30122 - OC-3/STM-1, OC-12/STM-4
- ZL30117 - OC-48/STM-16, OC-192/STM-64

Summary

- **ATCA provides suitable clocking features for carrier grade telecom network elements**
- **Consider using the RTM for BITS termination**
- **Centralized timing architecture provides an economical solution in systems with multiple line cards and provides for easy clock performance upgrade**
- **Distributed timing architecture economical for multi-functional systems that have limited slots requiring synchronization**