

“System in a Package” in the Medical Market

**Piers Tremlett,
Zarlink Semiconductor
NMI at TWI, 14 June 07**

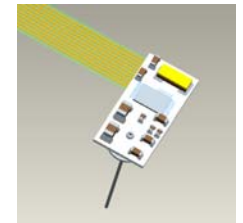
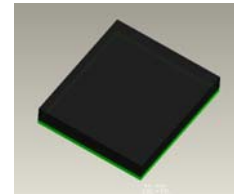
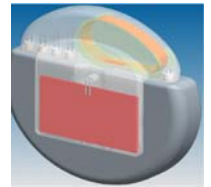


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Introduction



- Introduction to Zarlink Microelectronics (Caldicot, UK)
- In/on-body medical devices and pacemakers
- Zarlink's low power RF SiP modules
- Zarlink's SiP development
- The future for medical SiPs



Introduction to Zarlink Microelectronics



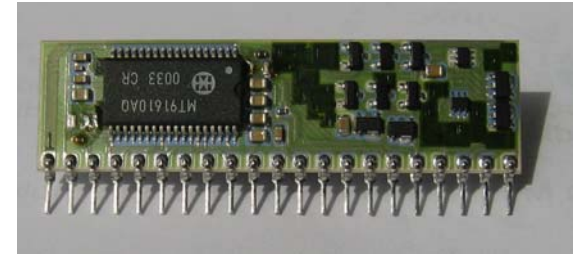
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Zarlink Microelectronics

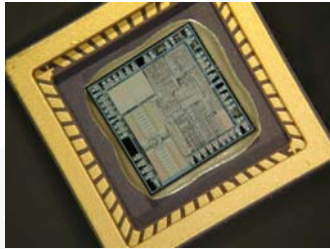
- **Packaging foundry**
 - 75% packages for implantable medical devices
 - 25% merchant subcontract packaging
- **Module and packaging design**
- **Based in Caldicot, South Wales**
- **75 employees**
- **Part of a multinational company – Zarlink Semiconductor**



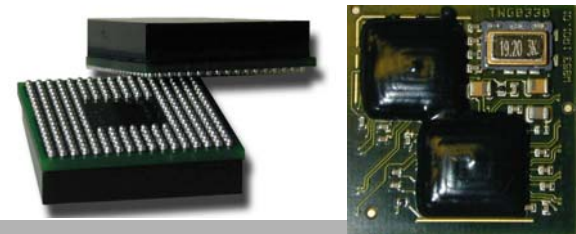
History



- **1980 established as manufacturer of ceramic hybrid circuits**
 - SLIC for telecom applications
- **2000 strategic decision to move into medical market**
- **2001 Medical Microelectronics packaging facility**



- **2003 1st SiP – Telecom timing module**



In/On-Body Medical Devices and the Pacemaker



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Examples Devices and Applications

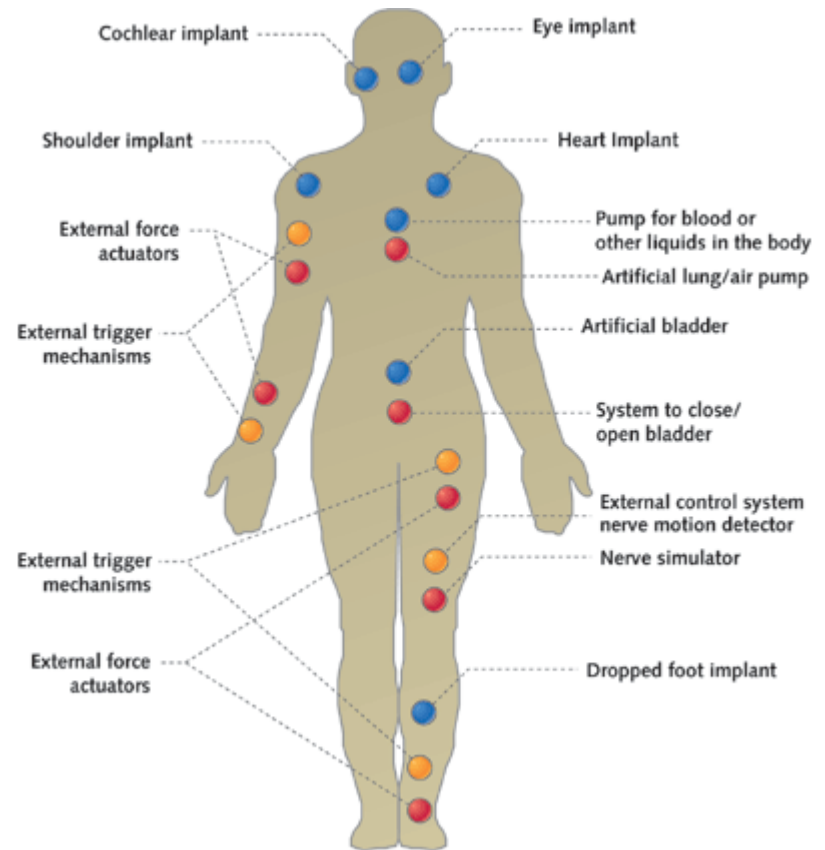
- Electronic devices treat these conditions

- **Profound Deafness**
Cochlear Implant

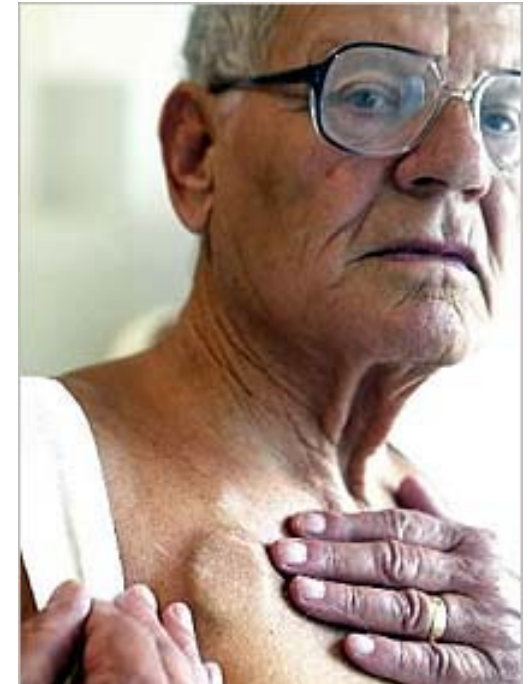
- **Heart conditions**
Pacemakers

- **Diabetes**
Insulin pumps

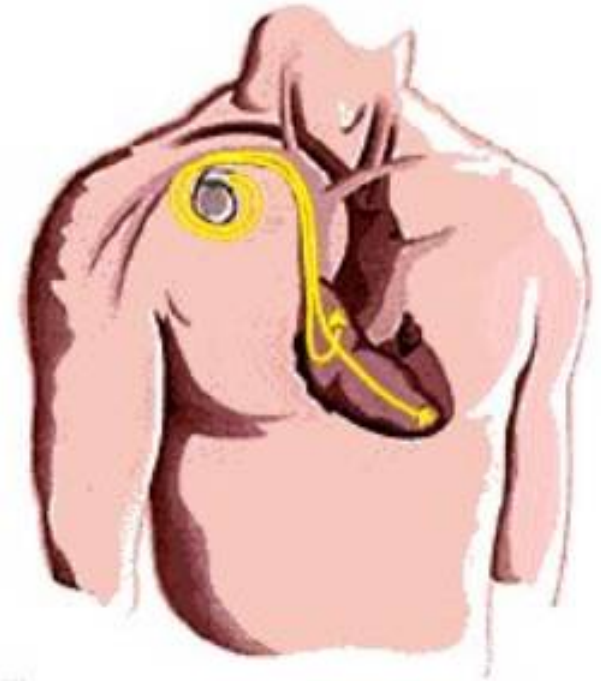
- **Paralysis**
Stroke victims
“Dropped Foot Implant”



Pacemakers



- **Implanted in shoulder under local**
- **Electrode lead into heart via vein**
- **Function: regulates and supplies missed heart beat pulses**
- **Operates seven years on one battery**
- **Entire pacemaker replaced**

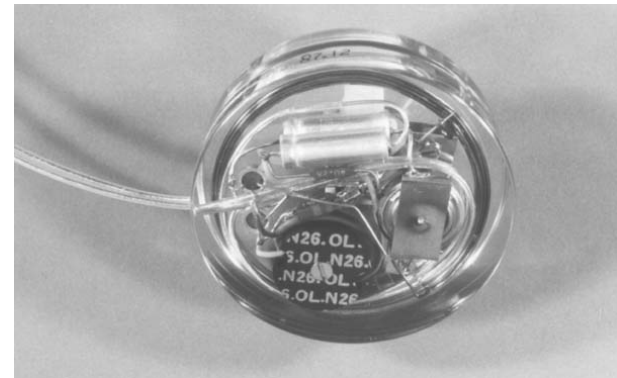


Pacemaker Case History

ARNE LARSSON



- ➔ Received first implantable heart pacemaker on October 8, 1958
- ➔ Died December 28, 2001 after 43 years with pacemaker
- ➔ Lived longer than the inventor of the pacemaker!



Zarlink's Low Power RF SiP Modules



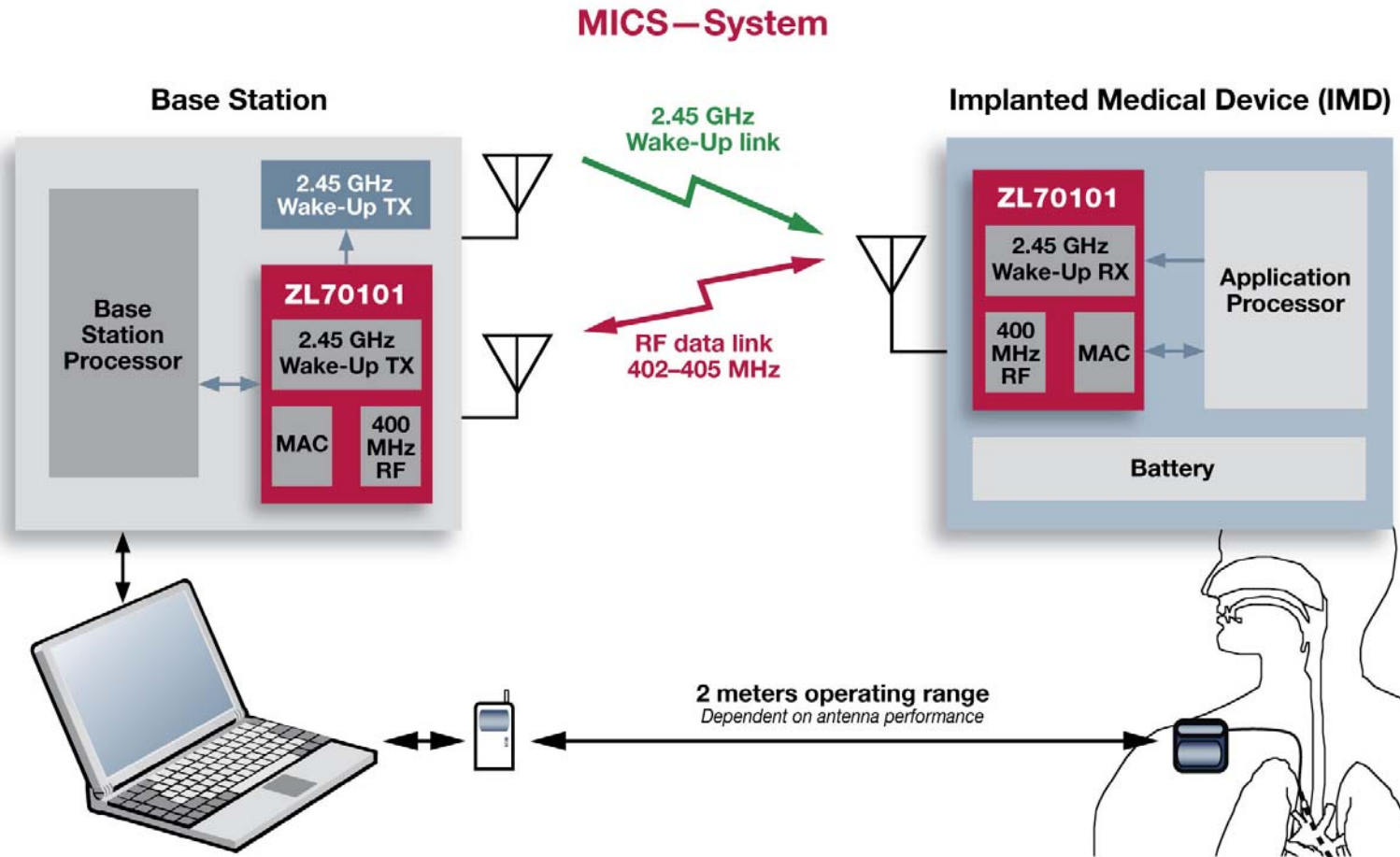
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Zarlink's Ultra Low-Power MICS Radio Chip

- **Zarlink Ultra Low Power Communications Group**
 - Based in San Diego, with design centre in Sweden
 - Design group for low power ICs
- **Pacemaker customers request RF link**
 - Short-range wireless link
 - Low power consumption
- **Zarlink produces SoC chip**
 - 5 μ A
 - 10 m range



Zarlink develops Ultra Low-Power Radio chip



MICS Benefits – Operating Room

Today



Future with MICS



- **Programming equipment can be located outside operating room, eliminating sterilization concerns with inductive coil communication during surgery**

MICS Benefits – Home Monitoring

Today



Future with MICS

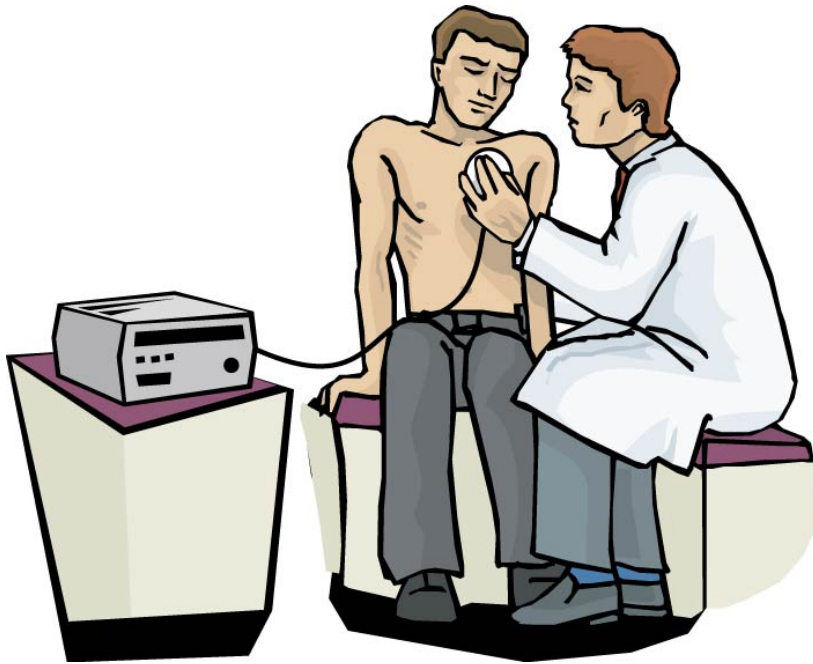


- Health and patient data transmitted wirelessly without requiring user intervention

MICS Benefits – Doctor's Office

Today

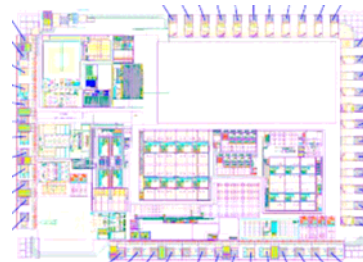
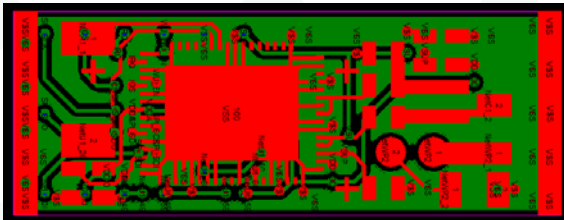
Future with MICS



- **Wireless link can be used to easily adjust therapy**

Zarlink's Radio Chip Leads To SiP

- **Zarlink IC exactly what customers want**
- **But to the IC design group's surprise**
 - Customer wanted an RF solution not a chip
- **S SiP module provides a solution**
 - If the RF did not work in the pacemaker, it was Zarlink's responsibility!
- **SiP suits Zarlink too**
 - Compliments SoC
 - provides flexibility for variants e.g. matching network
 - revenue per package rather than chip



Example of Zarlink's RF Medical SiP

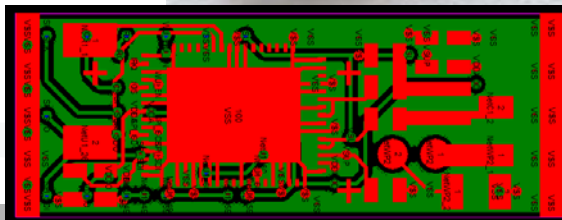
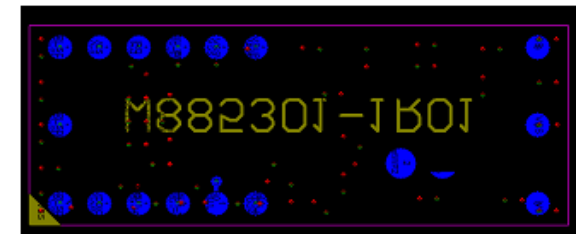
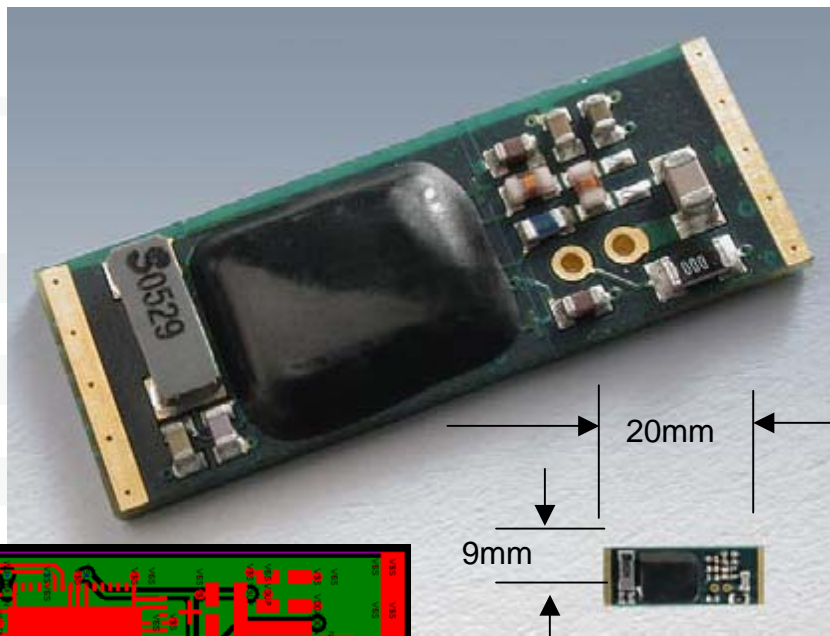
- **SiP advantage over SoC: delivered within 2 months**

Top side

Bottom side

Wire bonded die and SMT components

Ball grid array pads

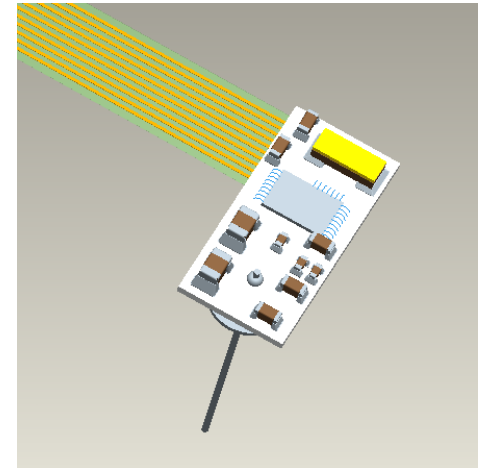


Customers Variants

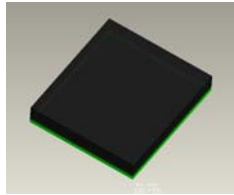
- **Different customer requirements:**

- HV protection
- ESD protection
- Antenna matching network
- Physical design

View inside can
(3D CAD picture)



Moulded SiP



Zarlink's SiP Development



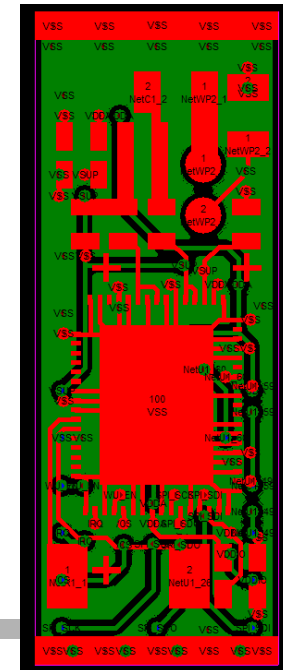
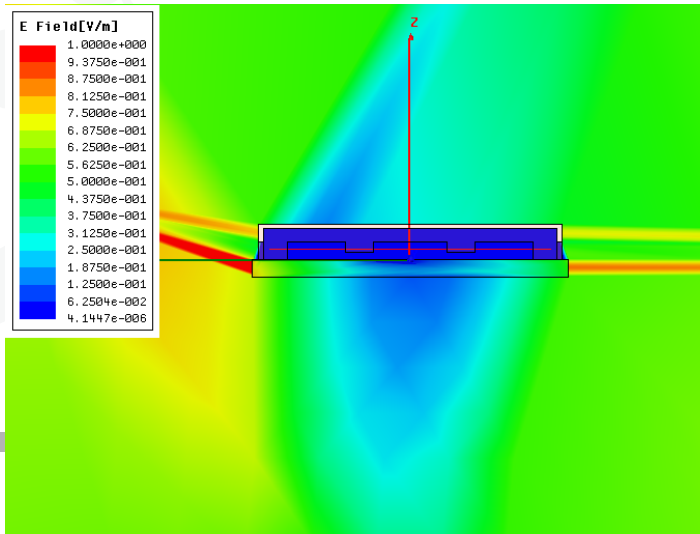
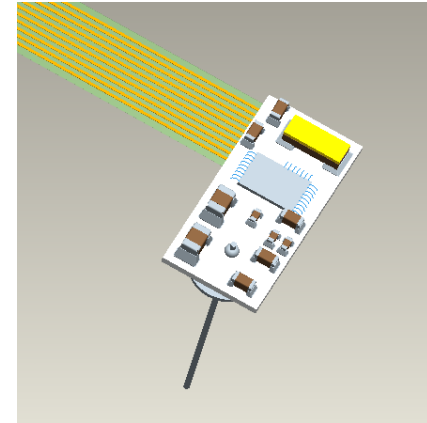
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Nature of Zarlink medical SiP projects

- **Usually multi-site and multi-national projects**
 - Large use of conference calls and Webex presentation tools
- **May include IC design**
- **Long project development times**
 - 2 – 3 years
- **Benefit from good project management**
 - Good product specifications
 - Good procedures
 - Able management

Design CAD Systems for RF SiP

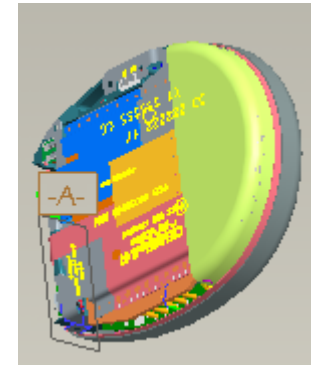
- **Extensive use of CAD systems**
- **3D CAD**
 - To present concepts
 - To ensure device fits customer's design
 - To provide drawings for components, e.g. shields
- **PCB layout**
 - To design PCB
- **RF/EMI simulation**
 - HFSS



Pacemaker Packaging Requirements Versus Mobile Phones

- **Aspects similar to mobile phone requirements**

- Smaller, slimmer pacemakers preferred by patients
- Additional features continually being added by suppliers
 - Defibrillation, exercise sensing
- Low-power consumption to preserve battery life
- RF communication



- **Differences from mobile phone packaging requirements**

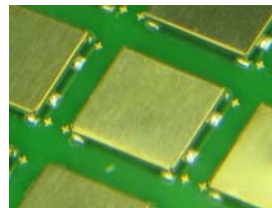
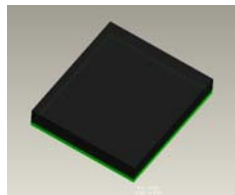
- Lower volumes
- Long design and approvals cycle
- Higher reliability



IC and package co development is essential

- **It pays to talk to Zarlink Microelectronics at the beginning of IC design...not the end!**
 - Less delay, cost and stress!
- **So, most functionality issues are are IC related...**
- **But.....**
 - Most reliability issues are package related
 - SiP packaging design rules: complex, interdependent and foundry specific
 - Thinking about SiP package during IC design helps:
 - Minimise package size
 - Improves package manufacturability and cost
 - Maximises SiP performance

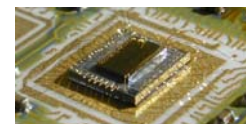
Find Out What Your Customer Wants: Overall Module Format and Pin Out



- **Package style**

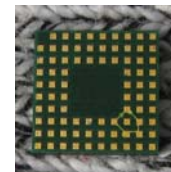
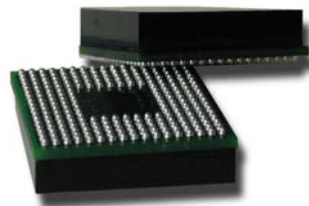
- Moulded/unmoulded
- Shield or not

- **Wire bond, flip chip, CSP or stacked die**



- **Interconnect style**

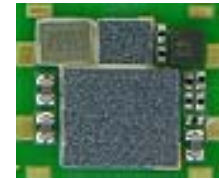
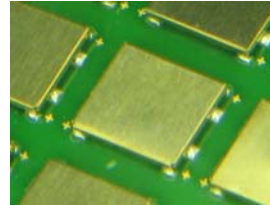
- BGA
- LGA
- Flex



Package Format

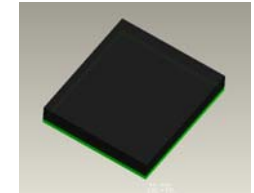
- **Shield/no shield**

- Provides -30dB attenuation
- Uses 22% of PCB space in SiP
- Problem of loss of shield during rework of SiP component?



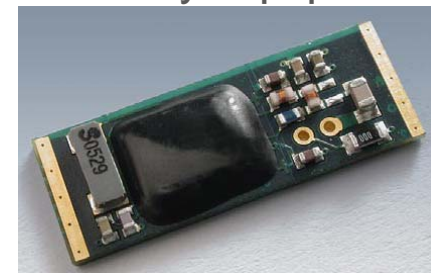
- **Moulding**

- Adds robustness e.g. reworkability
- Customer confidence and familiarity – SiP looks like an IC



- **Both**

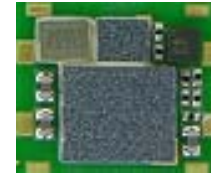
- Provide flat pick up surface for SMT component assembly equipment
- Surface for coding



Flip Chip, CSP, Wire Bond or Stacked Die

- **Flip chip / CSP**

- Lower parasitics, better density, more expensive
- Needs underfill (small CSP may be OK without)



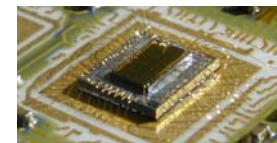
- **Wire bond**

- Higher parasitics, lower density, cheaper
- More common process

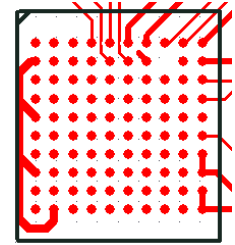


- **Stacked die**

- As for wire bond but more complicated
- But does have good density



Package Component Layout



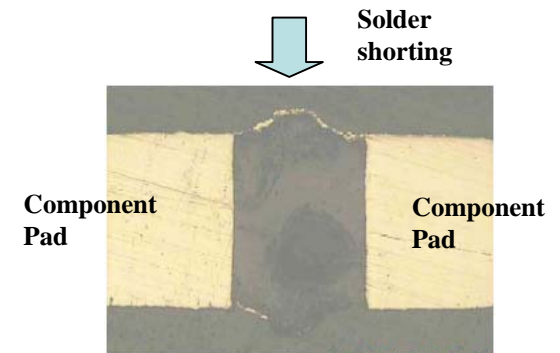
- **For co-design with new die or RDL design**

- Consider maximum designed die size and minimum future die shrink
- Design component layout with die pin out
- Jigsaw puzzle design for minimum size
- Earlier and more accurate simulation of package elements



- **Size and design rules**

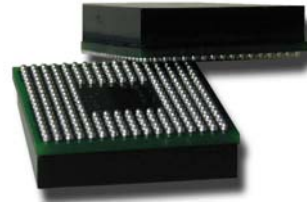
- Smallest possible format for components
 - Eg 0201 Surface Mount Technology (SMT) components (0.5mm x 0.25mm)
- Much tighter design rules than normal SMT
 - smaller component pads + tighter spacing
- Clearances for: wirebond tool, underfill flow
- Design to avoid solder extrusion



Interconnect Style

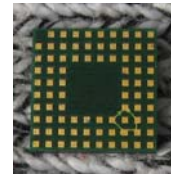
- **Ball Grid Array (BGA)**

- Tolerant to
PCB warpage
Thermal cycling / ceramic substrates



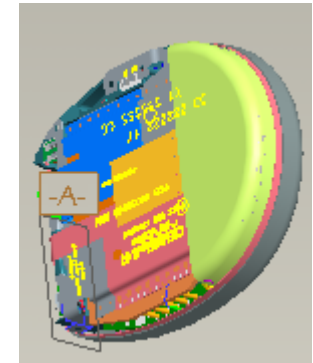
- **Leadless Grid Array (LGA)**

- Lower height format
- Less tolerant



- **Flex**

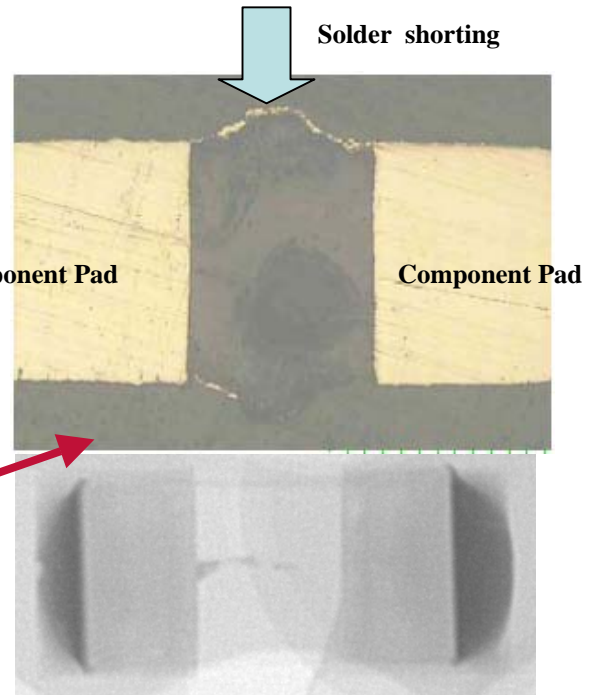
- Aids 3D assembly problems for pacemaker manufacturers



The Importance of the PCB

- **SiP tends to use a PCB rather than leadframe**
 - because it is a multi component package
- **Wire bond plating is complicated by SMT components**
 - They break track/bus bar continuity for gold electro plating
 - Also need to avoid Au embrittlement of solder joints
- **It is often a very demanding PCB for the PCB manufacturer**
 - PCB maybe 50% of package complexity
 - Would be nice if European suppliers could match Asian capabilities
- **Important to**
 - understand PCB manufacturing
 - Have a good PCB supplier – it is easy to be let down.

Co-Failure Analysis



- **Zarlink has good FA facilities**
- **SiP tends to be leading edge**
 - New failure modes
- **Important to allocate a failure cause**
 - to all development test sample fails
 - Immediately!
- **Most failures modes appear early but are ignored**
 - Resource / time pressure issues on failure analysis

The Future for Medical SiPs



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SiP in the Medical Market

- **Current implant usage of SiP is quite low**
- **Types of SiP used in implants**
 - Stacked die for memory/ logic integration
 - True SiP for RF modules
- **However, revenue for a SiP is 3x just the die**
 - A clear demand for SiP in certain applications
- **Note: totally integrated system packages are quite advanced**



“In the ear” hearing aid



Camera capsule

Will there be more medical SiP's?

- **Pacemakers are a large autonomous system**
- **Will they wish to modularise the contents?**
 - Diversification of applications similar to pacemakers: incontinence, Parkinsons
 - “Plug and play” functional block SiPs?
 - Already happening with some RF modules
- **Do they need to integrate more functionality and still shrink?**
 - Strong demand for smaller, lighter devices
- **Any circuit blocks that performance improvement with SiP?**
 - Currently only RF, possibly defibrillation or logic + memory
- **Future SiP use likely to increase**
 - Driven mainly by integration
 - Therefore likely to be stacked die packages

Future Project: Energy Harvesting

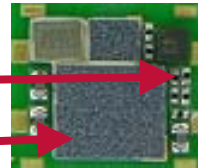
- **Desire to integrate more functionality**
 - Example, activity sensors
 - This is held back by energy usage
- **Size**
 - Battery is half the volume of a pacemaker
- **Zarlink is involved SIMM**
 - EU medical energy harvesting project
- **Will require small integrated energy management**
- **Another SiP application?**

Zarlink Continues SiP development

- **Development of subcontractors for high volume**

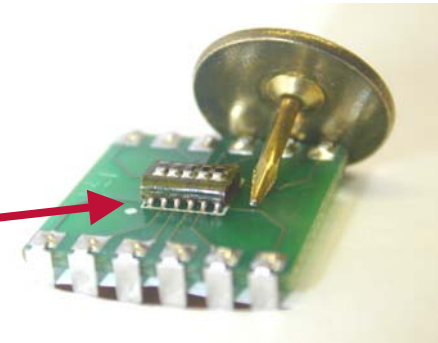
- **Improving internal capabilities**

- Smaller components eg 0201
- Flip chip – smaller pitch
- Stacked die



- **Investigating new packaging formats**

- Folded flex devices
- Embedded components



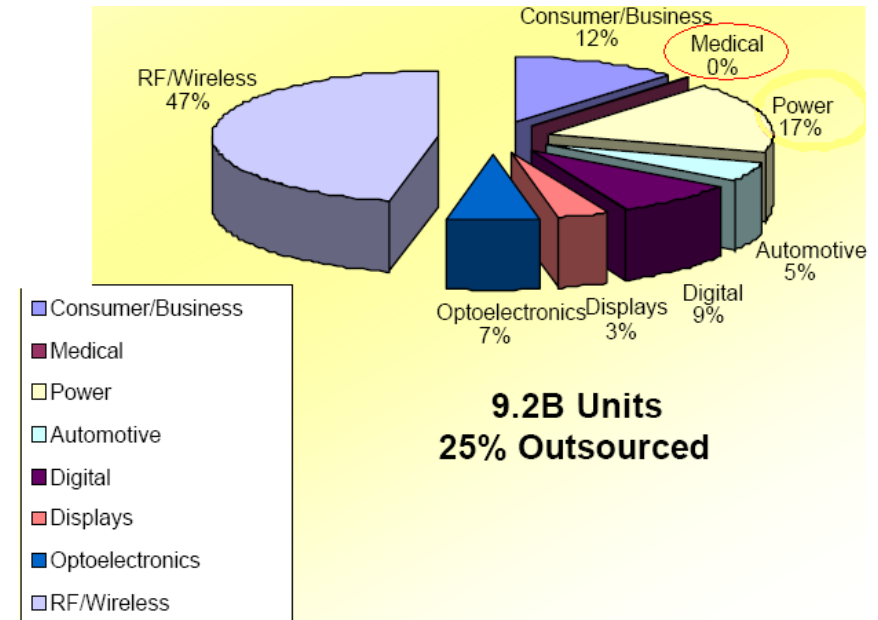
Convergence of PCB, SMT and Microelectronics

Moulding replaced by embedding of components in PCB lamination?

EU projects SHIFT and Adept

The Future for Medical Devices

- **No Market in 2002**
- **Demography and expectation**
 - Increasing elderly Western population
 - Expecting a healthy and active life
 - Rising health expectation in the East
- **Zarlink sees a steady growth in demand for medical SiPs**



SiP market size estimates
from Prismark 2002

ZARLINK SEMICONDUCTOR

